IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Guy B. Irving et al.
Serial No.:	08/848,816
Filing Date:	May 4, 2001
Group Art Unit:	2111
Examiner:	Khanh Nmn Dang
Title:	**SERVER CHASSIS HARDWARE MASTER SYSTEM AND METHOD**

MAIL STOP AMENDMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION PURSUANT TO 37 C.F.R. § 1.131

I, the undersigned, hereby declare and state that:

1. I am over the age of 21 years, of sound mind, and competent in all respects to make this Declaration.

2. I am an inventor of the subject matter of the above-referenced patent application, entitled *Server Chassis Hardware Master System and Method*, filed on May 4, 2001 (the "Application").

3. I was employed by Anigma, Inc. ("Anigma"), which was hired by RLX Technologies, Inc., the assignee of the Application (the "Assignee"), prior to July 12, 2000, to perform services related to a project entitled RLX Orbiter (the "Project"). As an employee of Anigma, I performed tasks relating to the Project and worked closely with employees of the Assignee.

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4. During the performance of my duties relating to the Project and prior to July 12, 2000, Guy B. Irving and I (the "Inventors") conceived the subject matter of at least Claims 1, 9, 10, 13, and 16 of the Application (the "Invention").

5. Beginning after conception of the Invention and prior to July 12, 2000, I participated in the design and creation of a single board server assembly and master circuitry program that incorporated the subject matter of the Invention. The single board server assembly and master circuitry program resulted in the completion of a prototype. The design and creation of the single board server assembly and master circuitry program and the completion of the prototype were ongoing endeavors to which I devoted a substantial portion of business hours beginning on a date before July 12, 2000 and continuing at least through July 23, 2000. The conception of the invention is further evidenced by a Specification entitled "Firmware Interface Specification Orbiter 1680, Orbiter 3360" that describes the subject matter of the invention, attached hereto as Exhibit A. The date of the Specification, which has been redacted for privacy reasons, is prior to July 12, 2000.

6. During the construction of the prototype, at least six versions of design schematics were completed before July 12, 2000, and included embodiments of the Invention. Attached as Exhibits B and C, respectively, are fifth and sixth versions of design schematics. The dates of the design schematics, which have been redacted for privacy reasons, are prior to July 12, 2000. The design schematics are each twenty-seven pages long and illustrate the complexity of the construction of the prototype.

7. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. Further, I declare that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

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Declaration pursuant to 37 C.F.R. § 1.131 in regard to 09/848,816.

Signed this 4 day of MARCH, 2005.

David M. Kirkeby

EXHIBIT A

[redacted]

[redacted]

Firmware Interface Specification
Orbiter 1680, Orbiter 3360

Table of Contents

1. SCOPE

This document defines the interface to the Orbiter devices that are accessible and or controllable by firmware or software.

This document also defines the operation of the BIOS that is unique to the Orbiter.

2. OVERVIEW

The Orbiter is a single board server. Up to two 2.5 inch hard drives or one 3.5 inch hard drive can be installed on the Orbiter PCBA.

Up to 24 Orbiters can be installed in a single specially designed enclosure (the HotDock Chassis).

The Orbiter uses a Transmeta processor (either the 3200 or the 5400). The Transmeta processors execute x86 type instructions. The Orbiter is a PC compatible type computer and most of the software interface on the Orbiter is compatible with standard PC design. The Orbiter includes some system monitoring and control devices that are not part of the standard PC architecture. The function of these devices and the interface to them are defined in detail in this document.

3. BIOS DESIGN

3.1. Original BIOS

The Orbiter BIOS is derived from the Phoenix ???? BIOS. This BIOS is a standard PC BIOS designed to run with the Transmeta 5400 and 3200 processors. This BIOS supports all current standard PC BIOS functionality including the following:

- Support for UltraDMA 66 IDE interface
- Support for boot from CD

3.2. Standard Features Not Part of Orbiter

The following devices are not part of the Orbiter. The BIOS may, but need not be designed to support these devices:

- Parallel Port
- USB Port
- Audio Codec
- Beeper
- Floppy Disk

3.3. Redirection of Display Output to Serial Port 1

The Orbiter BIOS redirects display I/O to serial port 1 when a display adapter is not detected. The default setup for Serial port 1 and serial port 2 is 38,400, 8 bits, no parity and no flow control.

3.4. LED indicators

The POST code results are displayed by blinking the Board Fault LED and Front Panel LED. The board good LED is turned on if the BIOS does not detect any problems. See the GPIO Output section for more details on the function of these LED's

3.5. LM87 Support

The Orbiter uses a National Semiconductor LM87 to monitor environmental status including voltages, fans and temperatures.

The BIOS sets up the LM87 limit registers as defined in this document so as to generate an SMB alert when a monitored parameter is out of range.

The BIOS loads status obtained from the LM87 into an extended DMI table.

The BIOS provides a mechanism for an external program to cause a DMI table refresh.

3.6. GPIO Table setup

Much of the South Bridge I/O has been redefined to support system monitor and control functionality. The BIOS provides the following functionality with regard to the GPIO ports.

- Sets up the ALI1535 I/O appropriately for the Orbiter functionality. See the GPIO Assignments for RLXORB section for details on the set up of the GPIO tables.
- Provides a call to allow the state of the input to a GPIO device used as an input to be determined.
- Provides a call to allow the state of the GPIO output to be set for a device used as an output.
- Provides a call to allow the interrupt generated by a GPIO to be hooked.

The GPIO port to be activated is referenced by its port number and not its function in the BIOS calls.

3.7.SMB Bus

The Orbiter SMB bus can access local SMB devices and System SMB devices. See the SMB (I^2C) Bus Addressing section for the addresses of the I^2C.

The Orbiter selects between the local and the system SMB bus using the signal, LOCAL_I2C_SEL. See the GPIO Assignments for RLXORB for details on this signal.

The BIOS provides access to the I^2C bus via a call.

All installed Orbiters can have access to the system I^2C bus. It is therefore necessary that this bus be accessed using I^2C multi-mastering techniques. It is desirable that if the system I2C bus is busy that the Orbiter reselect the local I^2C bus and wait about a millisecond before retrying the bus. This procedure will reduce the capacitive loading on the I^2C bus which will improve the reliability of communication on the system I^2C bus. It would also be desirable that a small additional time be added to the wait time based on the card slot. This procedure will eliminate the possibility of two devices preventing access for each other.

3.8. Watchdog timer

The ALI1535 contains a watchdog timer. The BIOS provides the hooks to enable the watchdog timer. The resident management program handles the watchdog timer if it is enabled to do so. The BIOS provides access to the environment monitor circuits by extending the DMI interface. In addition, the BIOS is extended to include support for a few control functions.

4. OVERVIEW GPIO INPUTS AND OUTPUTS

4.1. Inputs

Item	Description
Slot ID	6 bit code that indicates what slot this card is installed in
Power Supply Status	10 status lines (5 from each power supply) that indicates power supply status. See the Power Supply Status Lines section for more details on these signals.
Master/non-Master	A single GPIO input that indicates whether this card is installed in the master slot and therefore has master capability or not. See the Master Signal Function section for more details on the function of this signal.
Front Panel System Fault LED Control	The front panel system fault indicator enable line
Front Panel Board Fault LED Control	The front panel Orbiter board fault indicator enable line

4.2. GPIO Outputs (Excluding System Command Bus)

Item	Description
Board Fault LED (BRD_FAULT_LED)	Controls the state of the local board fault LED and the global board fault LED signal.
Board Good LED (BRD_GD_LED)	Controls the state of the board good LED.
Front Panel LED (ORB_LED)	Controls the state of the front panel LED for this board.
Fan High (FAN_HI)	Controls the high fan speed request line for this board.
Flash Write Enable (FLASHWE#)	Enables writing of the flash

4.3. System Command Bus

The Orbiter in the master slot can control the System Command Bus. The System Command Bus allows the Orbiter installed in the Master slot to send various commands to any other Orbiter.

The signals of this bus are as follows:

Item	Description
Slot Address (MBADD0_OUT to MBADD5_OUT)	This is the 6 bit address of the slot that the command is targeted for
Command (MBCMD0_OUT to MBCMD2_OUT)	This is a three bit bus that defines the command to be executed
Strobe (MBSTROBE_OUT#)	When this signal is driven low the targeted Orbiter executes the command. The strobe must be returned to a high to allow command completion

The commands are as follows:

Command	Description
000	Nothing happens. Intentially left as a no op to reduce possibility of an unintentional command
001	Causes a reset on targeted card
010	Causes the password interrupt line to be strobed
011	Causes a reset with CMDBUS_EVNT set
100	Cause the TST_BRD_PRES_IN# signal to go low
100 thru 111	Nothing happens. Reserved for future expansion

5. MASTER SLOT SIGNAL

Each Orbiter has an input pin that indicates if it is the "Master Computer". A computer that is the "Master" differs from all other Computers installed in the HotDock Chassis as follows:

- The System command bus is enabled to function for that computer.
- The Master input to the Master GPIO is high. This allows the system application to detect this and assign extended functionality to the "Master" computer.

The MASTER signal is high for only one device in the HotDock chassis. The logic for determining which device is "Master" is as follows:

- MASTER is always low for slots 3 through 24
- MASTER is always low for slots 1 and 2 if a Shelf Management Controller (SMC) is installed.
- MASTER is high for slot 1 if an SMC is not installed.
- MASTER is high for slot 2 if an SMC and a card in slot 1 is not installed.

6. RAM SIZING

There is no on board RAM. All RAM is in a single DIMM. The BIOS needs to poll this DIMM and set the RAM size appropriately.

7. CMS STORAGE

Transmeta recommends that the CMS code be stored in the BIOS ROM for production. Are there any Phoenix issues with this? Will RocketLogix handle the development of the binary BIOS image?

8. FAN SPEED CONTROL

Fan speed control will be implemented with a resident management program that polls the temperature inputs and determines whether it is safe to operate this card with a lower fan speed. If the resident management determines that it is safe the resident management program can set FAN_HI low. If all installed Orbiters set FAN_HI low the fan speed will be reduced to medium speed, otherwise the fan speed will be high.

9. POWER STATUS LINES

Each of the two power supplies has five status outputs. The definition of these status lines is:

Item	Description
PWOK	All DC outputs are within tolerance PWOK=HIGH indicates power OK This signal drives system fault LED control via an isolating diode.
ACOK#	AC input power is within expected range. A jumper on the LED board is installed to set the expected range to 200 to 240 VAC. If the jumper is not installed the expected range is 100 to 240 VAC. ACOK#=LOW indicates AC is ok
FAIL	A power supply failure has occurred. FAIL=HIGH power supply failure including fan has occurred.
PRFL	A power supply failure is predicted PRFL = HIGH indicates power supply is failing, Fan may not be functioning properly
PRESENT#	The power supply is present PRESENT#=LOW indicates supply is present

10. LM87 INFORMATION

10.1. LM87 Input Description

Item	Description
Fan Monitor	The tachometer output of the fan that is mounted in front of this Orbiter. Four slots share the same fan tachometer input.
Voltage	The voltage status of the LM87 for the CPU core voltage, 3.3 volts, 5 volts and 12 volts. The 2.5 volts is monitored via a general purpose analog input of the LM87.

Item	Description
Temperature	The two external and the one internal temperature monitors of the LM87. One of the external temperature sensors is part of the processor and the other is mounted at the front of the Orbiter to sense the input air temperature.
Chassis Intrusion	The front door is open

10.2. LM87 Limit Setup

These tables control when the LM87 will generate an SMB alert interrupt

Temperature Limits

TBD

Voltage Limits

TBD

Fan Speed Limits

TBD

10.3. LM87 Port Assignments

11. SMB (I^2C) BUS ADDRESSING

11.1. Local I^2C bus addressing

This table lists the I2C addresses of the devices that are on the Orbiter.

Device	Address
DIMM ID	TBD
LM87	0x2C
Orbiter ID	TBD
Clock Control Chip	0x69

11.2. System I^2C addressing

This table lists the I^2C addresses of the devices that could be detected via the system I^2C bus. Not all the boards listed in the table below are necessarily installed in a system. If a board is installed it will have a device ID EEPROM. It may not have status device.

Device	Address
HotDockChassis ID EEPROM (on the LED board)	0xA0
Hub Board device ID EEPROM	0xA2
Hub Status	0x40
Power Supply 1 device ID EEPROM	0xA4
Power Supply 2 device ID EEPROM	0xA6
I/O Slot 1 device ID EEPROM	0xA8
I/O Slot 1 Status	0x48
I/O Slot 2 device ID EEPROM	0xAA

Device	Address
I/O Slot 2 Status	0x4A
I/O Slot 3 device ID EEPROM	0xAC
I/O Slot 3 Status	0x4C
I/O Slot 4 device ID EEPROM	0xAE
I/O Slot 4 Status	0x4E

12. SMB ALERT INTERRUPT

If the BIOS detects an SMB alert interrupt from the LM87 or the ALI1535 the BIOS will do the following.

If the interrupt was generated as the result of a fault the BIOS will set board fault LED. The BIOS will log the fault in its event log

Question: who (BIOS or resident management program) and under what conditions should the board fault LED be reset?

Question: Does system status data cause any kind of interrupt event?

13. ID SERIAL EEPROM CONTENTS DESCRIPTION

14. DMI TABLE DATA

15. CLOCK GENERATOR SETUP

16. PCI SLOT ASSIGNMENTS

Component	REQ	GNT	INT	PCI ID	Notes
PCI Slot for debug	0	0	PIRQ0#	AD16	DEBUG Only
LAN Public	1	1	PIRQ1#	AD20	82559ER
LAN Private	2	2	PIRQ2#	AD21	82559ER
LAN Management	3	3	PIRQ3#	AD22	82559ER
ALI 1535 Main				AD18	
ALI 1535 PMU				AD28	
ALI 1535 IDE				AD27	
ALI 1535				AD31	Not used in this

USB					design
ALI 1535 Audio				AD17	Not used in this design
ALI 1535 Modem				AD19	Not used in this design

17. FLASH PROGRAMMING

The Orbiter will support remote BIOS updates.

The embedded programming algorithms support the following Flash parts:

Part Number	Manufacturer
AMD29F160DT120EC	AMP

18. HARD DISK STARTUP

It is generally a good idea to sequence the start up of the hard disks to reduce the total startup current. It is imperative that hard drive start up be sequenced for Twenty four board systems that have two drives installed on more than half the cards.

19. HUB BOARD STATUS MONITORING

20. 485 BUS

The HotDock Chassis has a 485 Bus connected to each Orbiter and to the SMC slot. This is a half duplex 485 type bus.

The Orbiter can communicate through this bus using its COM2 port. The receive side is always enabled. The transmit side is enabled by raising the COM2 RTS.

The bus can either be used as a polled bus with a single computer serving as the master (probably the computer with the MASTER signal high). Or the bus can be used for multi-drop communication. If this approach is used it is up to the application to appropriately detect and recover from collisions.

21. GPIO ASSIGNMENTS FOR RLXORB

21.1. Outputs

SIGNAL NAME	FUNCTION	GPIO PIN	Default Type	PIN #	Voltage	State After BIOS Init
FAN_HI	0=Fan LOW 1=Fan HIGH	SCLK/PDMA_REQ#/RUN_ENT14, GPIO14	I	E4	3.3v/5v IN 5v OUT	GPO, HIGH
BRD_FAULT_LED	0=LED Off 1=LED On	FANOUT1/RUN_ENT8/GPIO8	0,H	W5	3.3v/5v IN 5v OUT	GPO, (note 1)
BRD_GD_LED	0=LED On 1=LED Off	RUN_ENT0/GPIO0	I	Y3	3.3v/5v IN 5v OUT	GPO, (note 2)
ORB_LED	0=LED Off 1=LED On	FANIN2/GPOI9	I	Y5	3.3v/5v IN 5v OUT	GPO, (note 3)
FLASHWE#	0=Enable Write to Flash 1=Flash Write Protected	FANOUT2/RUN_ENT8/GPIO8	0,H	V5	3.3v/5v IN 5v OUT	GPO, HIGH
LOCAL_I2C_SEL	0=System I2C selected 1=Local I2C selected	ACGP_UP#/RUN_ENT11/ GPIO11	IPH	U3	3.3v/5v IN 5v OUT	GPO, HIGH

Note 1 - The BIOS sets this output to HIGH when it initiates the GPIO ports. The BIOS sets this output to LOW when POST exits if an error was not detected. The BIOS causes this output to flash the POST result if an error was detected.

Note 2 – The BIOS sets this output to HIGH when it initiates the GPIO ports. The BIOS sets this output to LOW to when POST exists if an error was not detected.

Note 3 – The BIOS sets this output to HIGH when it initiates the GPIO ports. The BIOS sets this output to LOW when POST exits if an error was not detected. The BIOS causes this output to flash the POST result if an error was detected.

Command Bus
The BIOS sets these ports to Outputs. The signals are buffered and disabled on every board unless the master signal is active for the slot the board is installed in.

SIGNAL NAME	FUNCTION	GPIO PIN	Default Type	PIN #	Voltage	Pin type and state after BIOS init
MBADD0_OUT	Management Bus address 0	HDSEL#/RUN_ENT19/EGPIO3	O	M19		GPO, LOW

MBADD1_OUT	Management Bus address 1	ACGP_DOWN#/RUN_ENT12/ GPIO12	IPH	R5	3.3v/5v IN 5v OUT	GPO, LOW
MBADD2_OUT	Management Bus address 2	ACGP_MUTE#/RUN_ENT13/ GPIO13	IPH	U2	3.3v/5v IN 5v OUT	GPO, LOW
MBADD3_OUT	Management Bus address 3	DENSEL/EGPIO14	O	J19	3.3v/5v IN 5v OUT	GPO, LOW
MBADD4_OUT	Management Bus address 4	ACGAME [6], GPIO18	IPH	Y1	3.3v/5v IN 5v OUT	GPO, LOW
MBADD5_OUT	Management Bus address 5	LFRAME#/RUN_ENT5, GPIO5	O	N20	3.3v/5v IN 5v OUT	GPO, LOW
MBCMD0_OUT	Management Bus command line 0	LDRQ#/RUN_ENT4, GPIO4	I	P17	3.3v/5v IN 5v OUT	GPO, LOW
MBCMD1_OUT	Management Bus command line 1	ACGAME [2], GPIO16	I	V3	3.3v/5v IN 5v OUT	GPO, LOW
MBCMD2_OUT	Management Bus command line 2	ACGAME [3], GPIO17	I	W1	3.3v/5v IN 5v OUT	GPO, LOW
MBSTROBE_OUT #	Management Bus strobe	MOT1#/GPIO10	O/HI	K18	3.3v/5v IN 5v OUT	GPO, HIGH

21.2. Inputs

SIGNAL NAME	FUNCTION	GPIO PIN	Def Type	PIN #	Voltage	Notes
MASTER	0=This board is not master 1=This board is master	WPROT#/EGPIO11	IPH	M16	3.3v/5v IN 5v OUT	GPI
PASSWRDRST#	0=Password Reset Button Pushed 1=Normal	RUN_ENT1/GPIO1	I	V4	3.3v/5v IN 5v OUT	GPI, Interrupt
SLOTID0	Board ID 0	FD_DIR#/EGPIO4	O	L16	3.3v/5v IN 5v OUT	GPI
SLOTID1	Board ID 1	STEP#/EGPIO5	O	L17	3.3v/5v IN 5v OUT	GPI
SLOTID2	Board ID 2	WGATE#/EGPIO1	O	L19	3.3v/5v IN 5v OUT	GPI
SLOTID3	Board ID 3	DRV0#/EGPIO7	O	K19	3.3v/5v IN 5v OUT	GPI

SIGNAL NAME	FUNCTION	GPIO PIN	Def Type	PIN #	Voltage	Notes
SLOTID4	Board ID 4	DRV1#/EGPIO8	O	K20	3.3v/5v IN 5v OUT	GPI
SLOTID5	Board ID 5	MOT0#/EGPIO9	O	K17	3.3v/5v IN 5v OUT	GPI
PSACOK1#	0=Power Supply 0 AC OK 1=Power Supply 0 AC Not OK	RDATA#/EGPIO0	I	M18	3.3v/5v IN 5v OUT	GPI
PSACOK2#	0=Power Supply 1 AC OK 1=Power Supply 1 AC Not OK	PCMDATA/RUN_ENT10, GPIO10	IPH	T3	3.3v/5v IN 5v OUT	GPI
PSFAIL1	0=Normal 1=Power Supply 0 Failure	GPI24	I	M17	3.3v/5v IN	GPI
PSFAIL2	0=Normal 1=Power Supply 1 Failure	GPI25	I	E9	3.3v/5v IN	GPI
PSPRESENT1#	0=Power Supply 0 Present 1=Power Supply 0 Not Present	OVCR0#/GPIO20	IPH	T5	3.3v/5v IN 5v OUT	GPI
PSPRESENT2#	0=Power Supply 1 Present 1=Power Supply 1 Not Present	OVCR1#/GPIO21	IPH	T6	3.3v/5v IN 5v OUT	GPI
PSPWROK1	0=Power Supply 0 Power OK 1=Power Supply 0 Power Not OK	OVCR2#/GPIO22	IPH	U5	3.3v/5v IN 5v OUT	GPI
PSPWROK2	0=Power Supply 1 Power OK 1=Power Supply 1 Power Not OK	OVCR3#/GPIO23	IPH	U6	3.3v/5v IN 5v OUT	GPI
PSPRFAIL1	0=No power supply fail predicted 1=Power supply fail predicted	DSKCHG#/EGPIO6	I	M20	3.3v/5v IN 5v OUT	GPI
PSPRFAIL2	0=No power supply fail predicted 1=Power supply fail predicted	LRCLK/PDMA_GNT#/RUN_ENT15, GPIO15	I	E5	3.3v/5v IN 5v OUT	GPI
FLASHRDY#	0=Flash Busy 1=Flash Ready	ACGAME[7],GPIO19	I	Y2	3.3v/5v IN 5v OUT	GPI
IDECDP	Cable detect for 66mhz UDMA primary 80pin	AGP_BUSY#/GPI26/CBLID_P	I	D11	3.3v/5v IN	CBLID_P
IDECDS	Cable detect for 66mhz UDMA secondary 80 pin	AGP_STP#/GPO33/CBLID_S	I	E11	3.3v/5v IN	CBLID_S

SIGNAL NAME	FUNCTION	GPIO PIN	Def Type	PIN #	Voltage	Notes
BRD_FAULT#	0=Board fault exists in system 1=No board faults in system	TRK0#/EGPIO12	IPH	L20	3.3v/5v IN 5v OUT	GPI
SYS_FAULT#	0=System fault exists 1=No board faults	INDEX#/EGPIO13	IPH	J20	3.3v/5v IN 5v OUT	GPI
CMDBUS_EVNT	0=no command bus event 1= command bus event present	RUNENT2/GPIO2	I	W4	3.3v/5v IN 5v OUT	GPI, Interrupt Output of command bus decode
TST_BRD_PRES_IN#	0=Orbiter responded to command bus present query 1=no response to command bus query	RUNENT3/GPIO3	I	Y4	3.3v/5v IN 5v OUT	GPI This signal is read by MASTER computer only

21.3. Spares

GPIO PIN	Def Type	PIN #	Voltage	Notes
WGATE#/RUN_ENT18/EGPIO2	O	L18	3.3v/5v IN 5v OUT	
SLOWDOWN/GPIO21 (not available when ovcr1# used for GPIO21)	O	D9	3.3v/5v IN 3.3V OUT	GPIO21 is being used so this isn't really a spare

EXHIBIT B

Released Rev. A.5 (000621.1040)

Anigma Inc.

Title: RLXORB

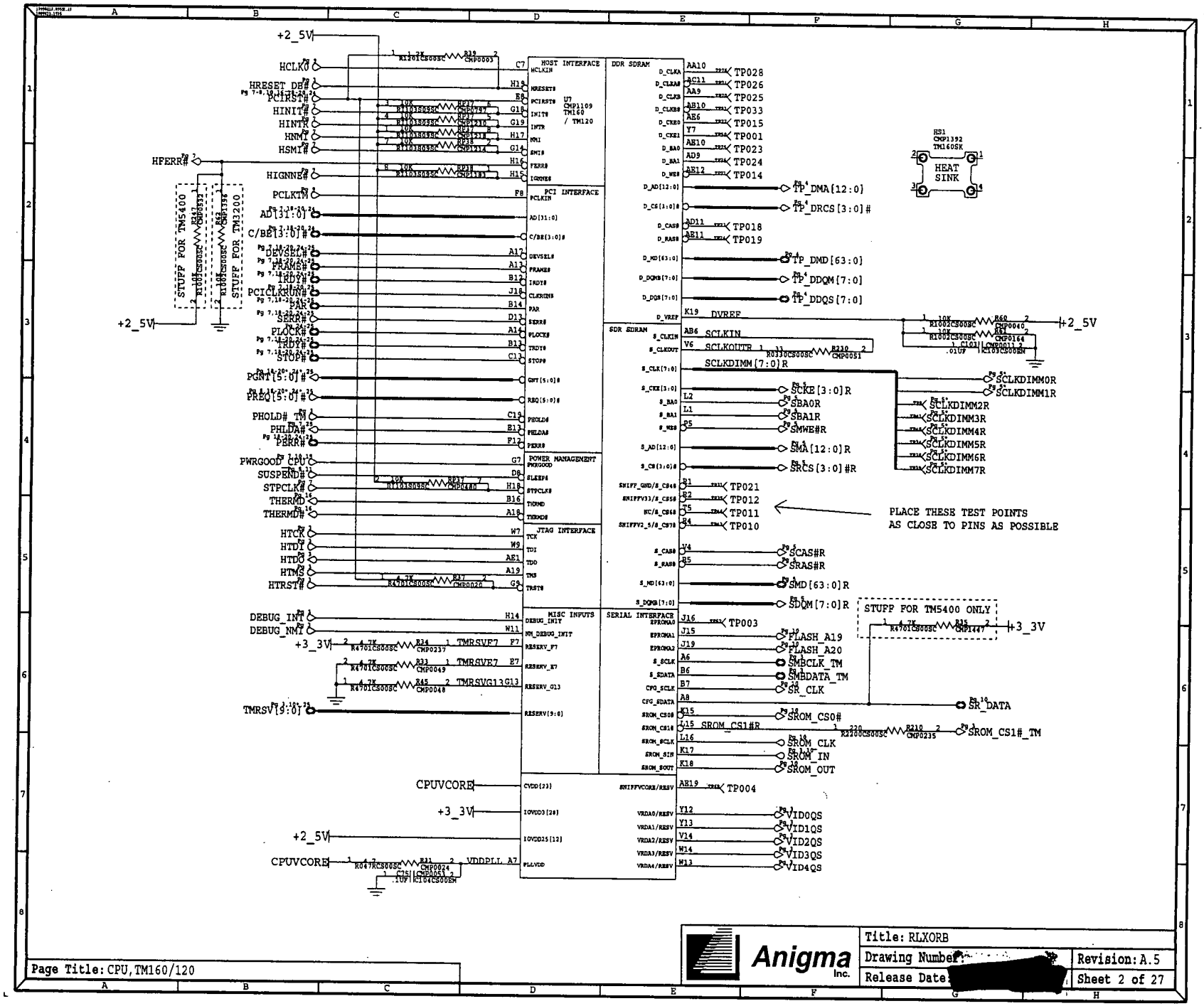
Drawing Number:

Revision: A.5

Release Date [redacted]

Sheet 1 of 27

Page Title: Index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DDR SDRAM
SDR SDRAM
POWER MANAGEMENT
JTAG INTERFACE
MISC INPUTS
SERIAL INTERFACE
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HFERR#
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IRDY#
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STOP#
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PHLDA#
PERR#
PWRGOOD_CPU
SUSPEND#
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THERMD#
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HTDI
HTDO
HTMS
HTRST#
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CPUVCORE
VDDPLL
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D_CLKB
D_CLKB#
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D_BA1
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D_RAS#
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NC/S_CS6#
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EPROMA2
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VID2QS
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VID4QS
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TP021
TP023
TP024
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TP014
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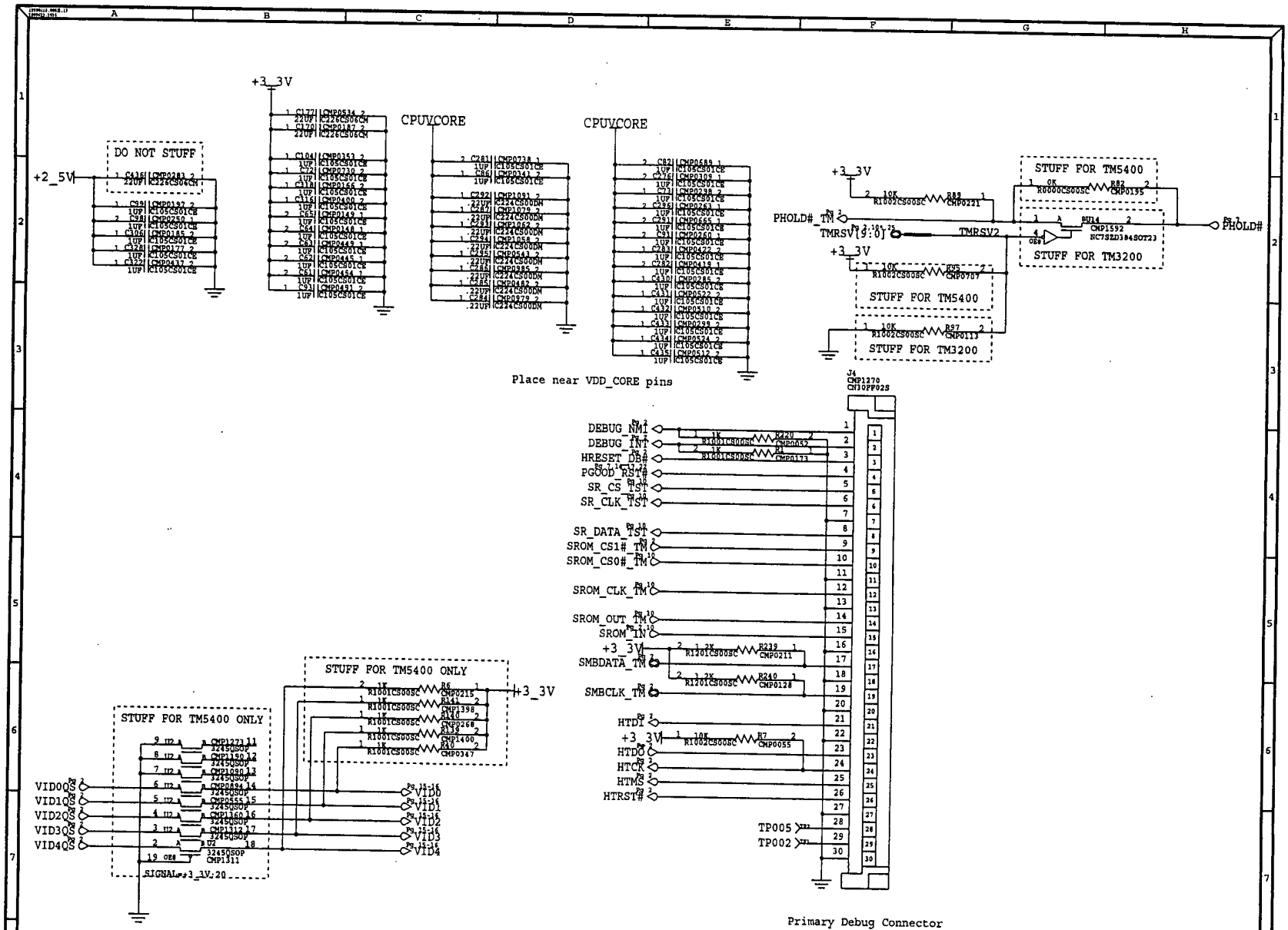
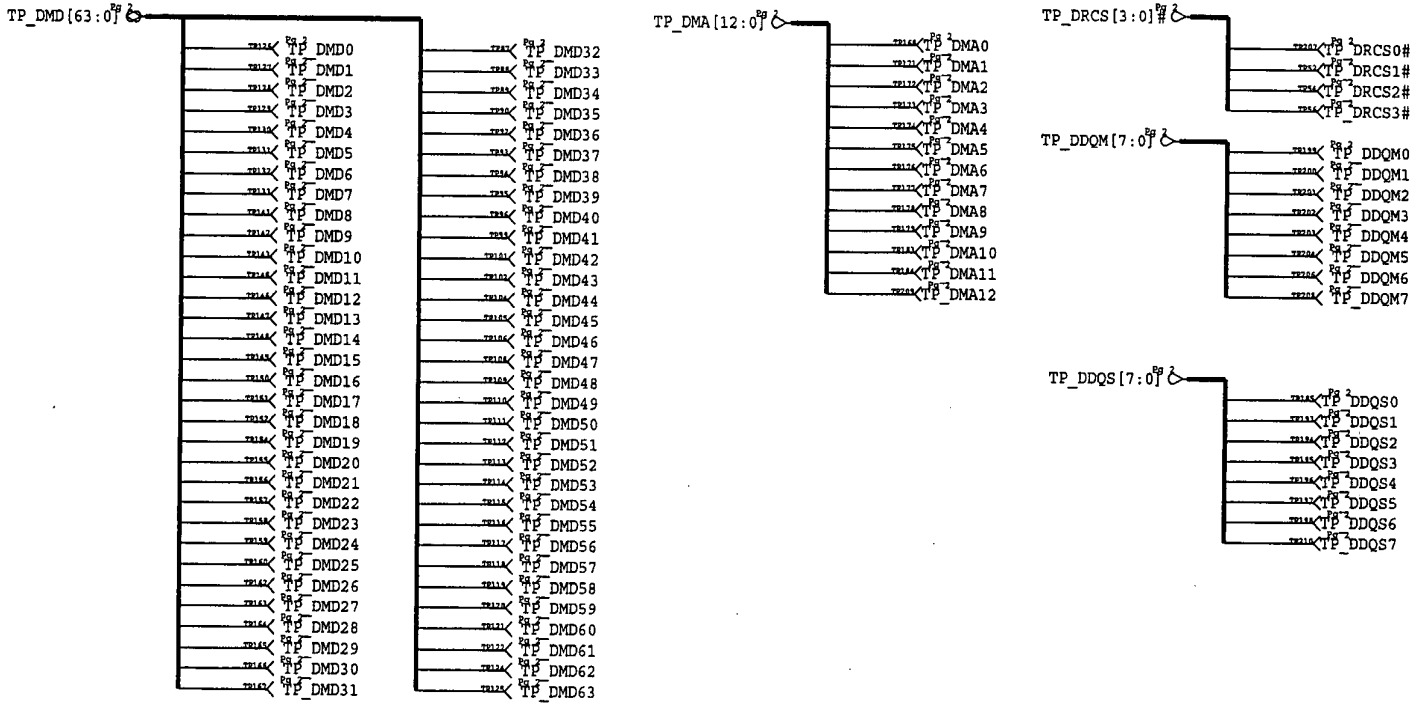
SCLKDIMM0R
SCLKDIMM1R
SCLKDIMM2R
SCLKDIMM3R
SCLKDIMM4R
SCLKDIMM5R
SCLKDIMM6R
SCLKDIMM7R
PLACE THESE TEST POINTS
AS CLOSE TO PINS AS POSSIBLE
STUFF FOR TM5400 ONLY
STUFF FOR TM5400
STUFF FOR TM3200
HEAT SINK
+2_5V
+3_3V
TMRSVE7
TMRSVG13
Page Title: CPU,TM160/120
Anigma Inc.
Title: RLXORB
Drawing Number: [redacted]
Revision: A.5
Release Date: [redacted]
Sheet 2 of 27

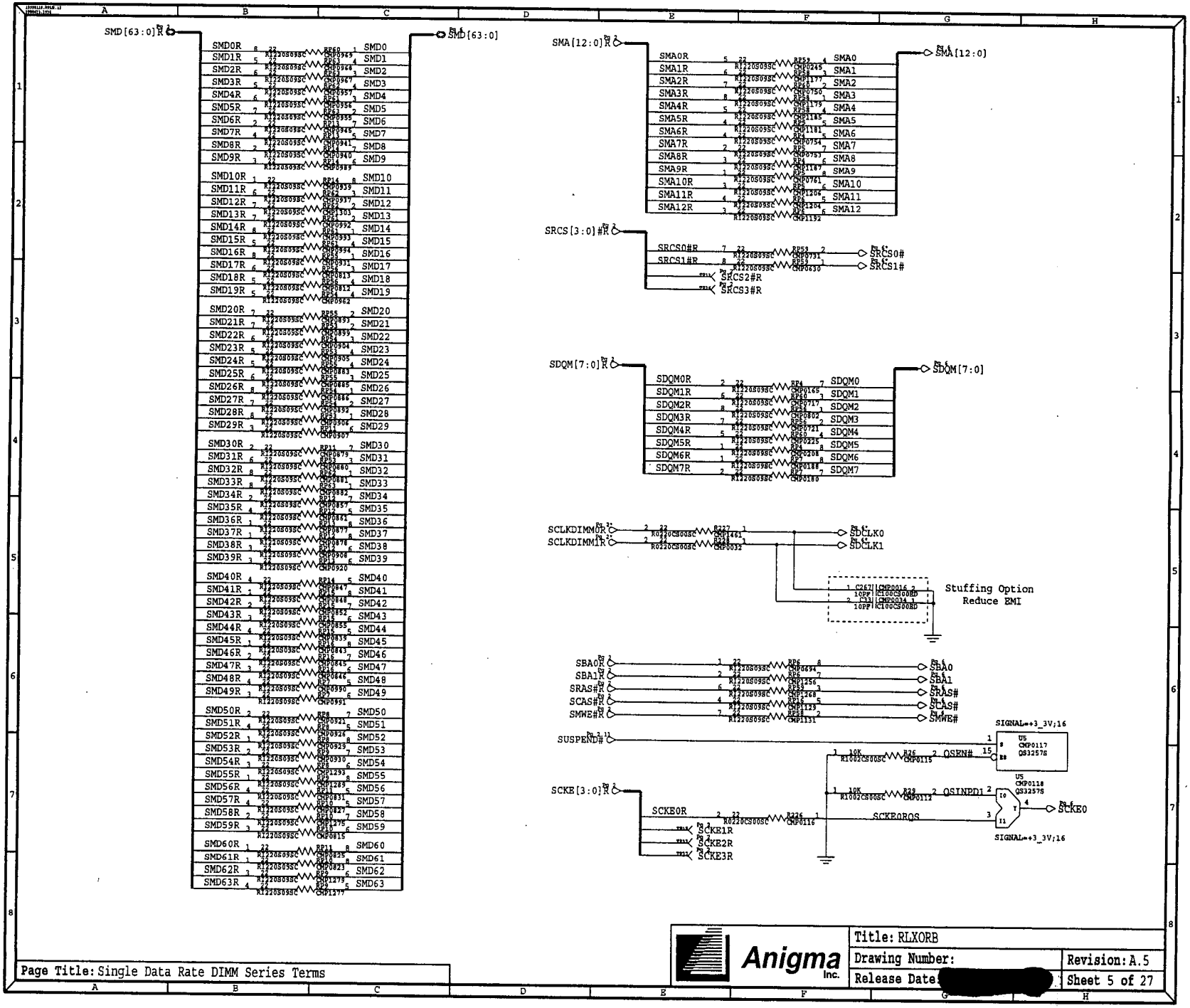

+3_3V
CPUVCORE
CPUVCORE
DO NOT STUFF
+2_5V
Place near VDD_CORE pins
+3_3V
PHOLD# TM
TMRSV[3:0]
TMRSV2
PHOLD#
STUFF FOR TM5400
STUFF FOR TM3200
STUFF FOR TM5400
STUFF FOR TM3200
DEBUG_NMI
DEBUG_INT
HRESET_DBA
PGOOD_RST#
SR_CS_TST
SR_CLK_TST
SR_DATA_TST
SROM_CS1# TM
SROM_CS0# TM
SROM_CLK_TM
SROM_OUT_TM
SROM_IN
+3_3V
SMBDATA_TM
SMBCLK_TM
HTDI
+3_3V
HTDO
HTCK
HTMS
HTRST#
TP005
TP002
STUFF FOR TM5400 ONLY
STUFF FOR TM5400 ONLY
+3_3V
VID0
VID1
VID2
VID3
VID4
VID0Q
VID1Q
VID2Q
VID3Q
VID4Q
SIGNAL +3_3V: 20
Primary Debug Connector
Anigma Inc.
Title: RLXORB
Drawing Number:
Release Date:
Revision: A.5
Sheet 3 of 27
Page Title: TM debug Port, Decoupling,ect...



Page Title: Test points for unused DDR pins

Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.5
Release Date [redacted]	Sheet 4 of 27



Page Title: Single Data Rate DIMM Series Terms

Anigma Inc.

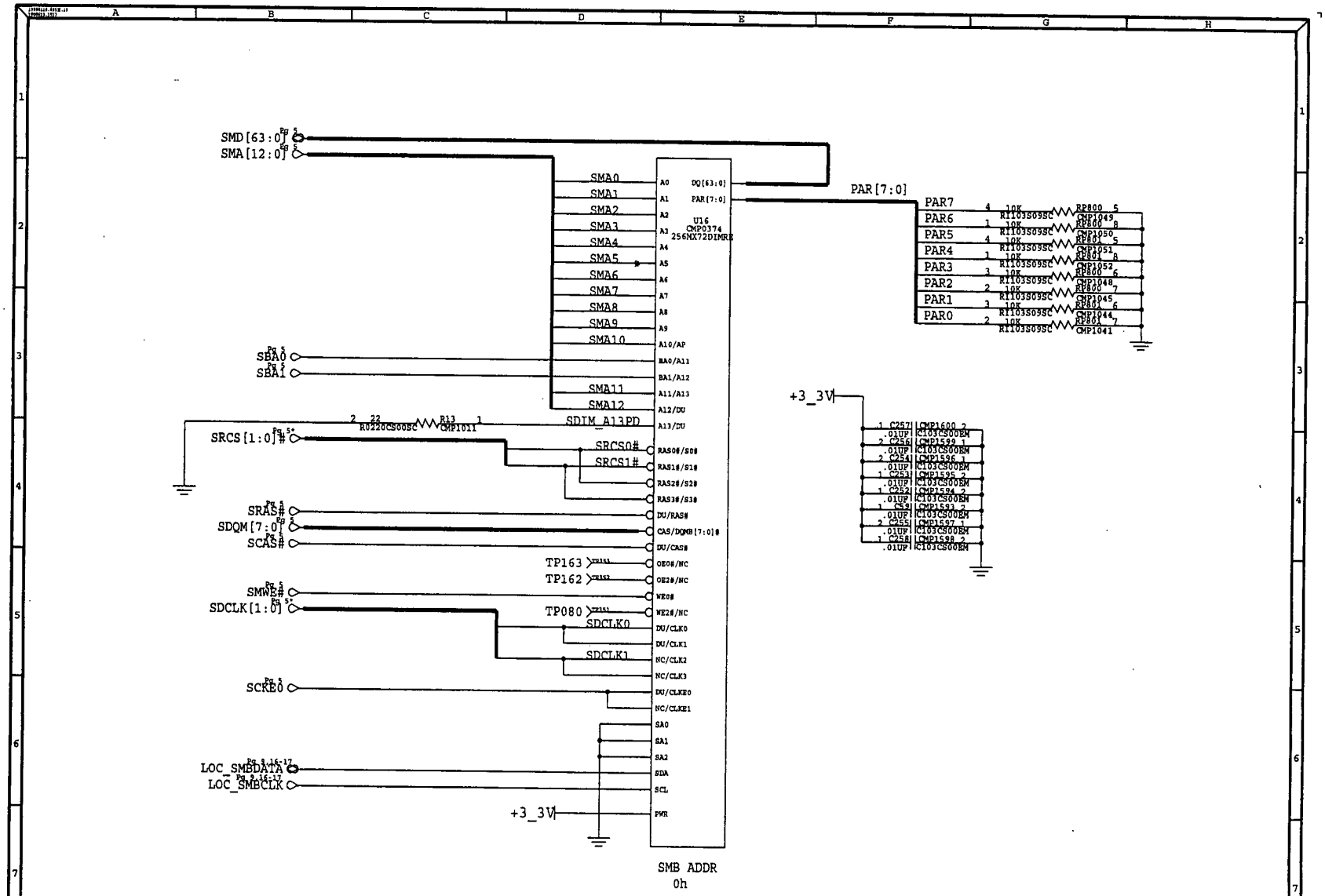
Title: RLXORB

Drawing Number:

Revision: A.5

Release Date: [redacted]

Sheet 5 of 27



Page Title: DIMM Module

Anigma Inc.

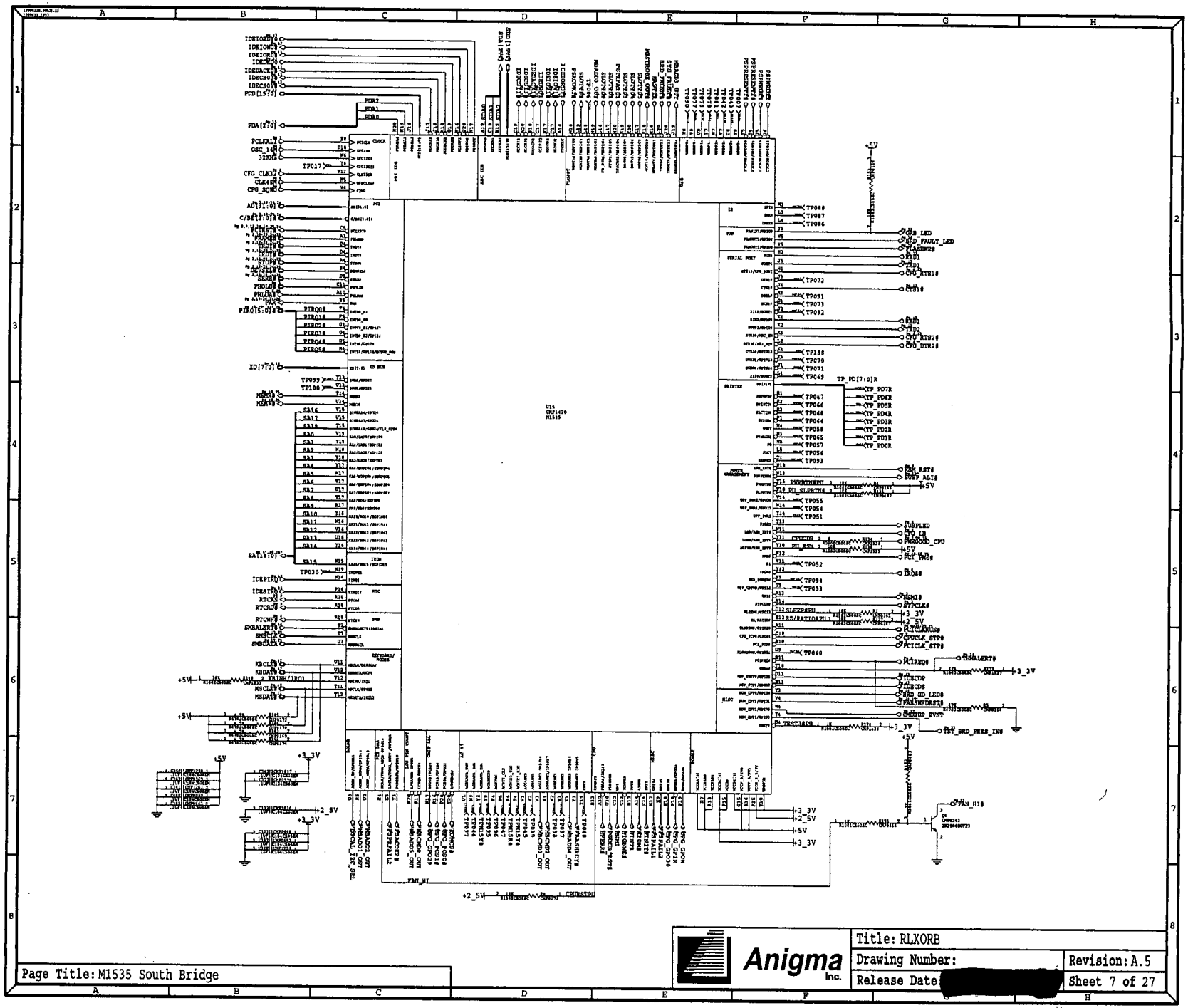
Title: RLXORB

Drawing Number:

Release Date [redacted]

Revision: A.5

Sheet 6 of 27



Page Title: M1535 South Bridge

Anigma Inc.

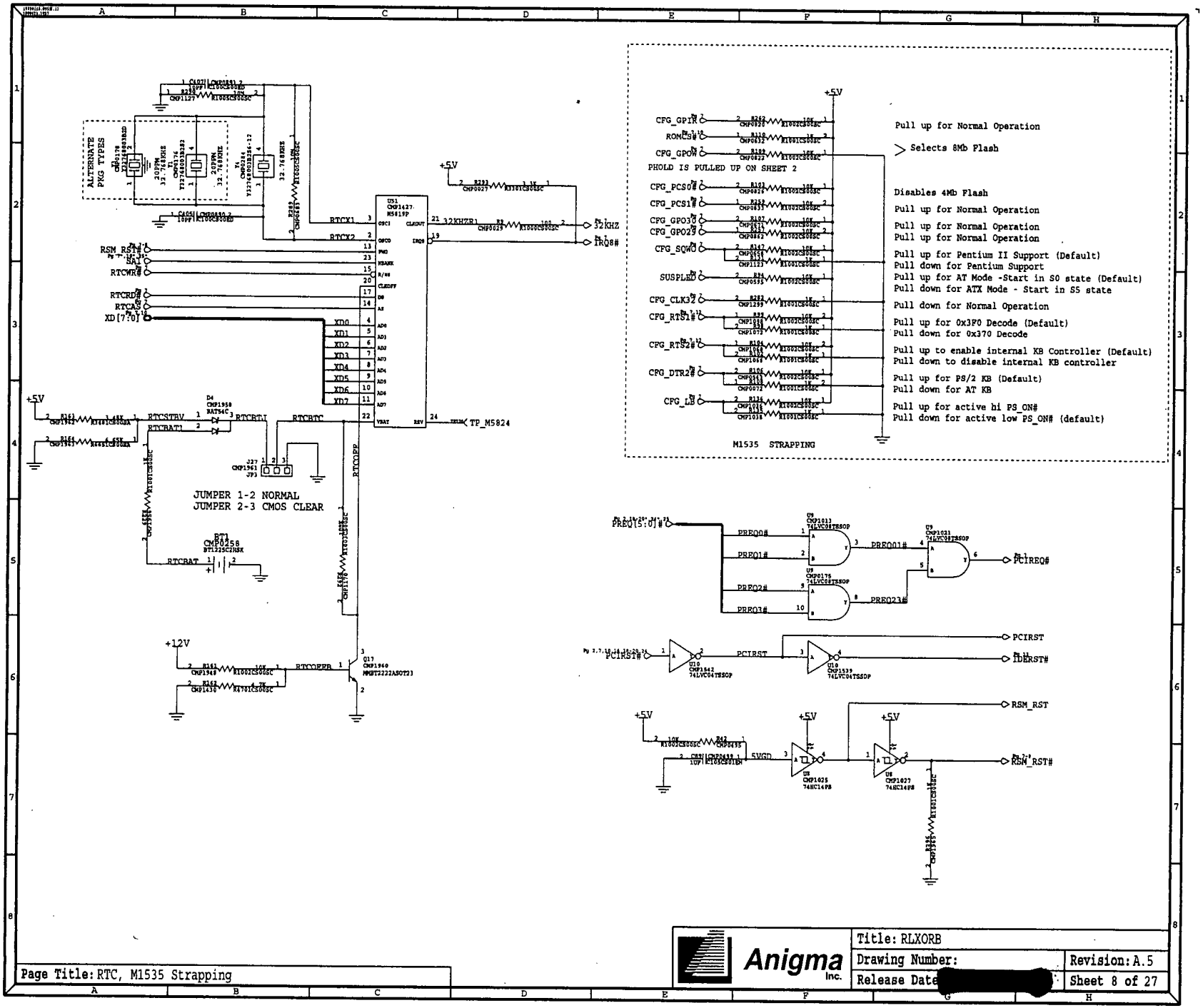
Title: RLXORB

Drawing Number:

Revision: A.5

Release Date: [redacted]

Sheet 7 of 27



Page Title: RTC, M1535 Strapping

Anigma Inc.

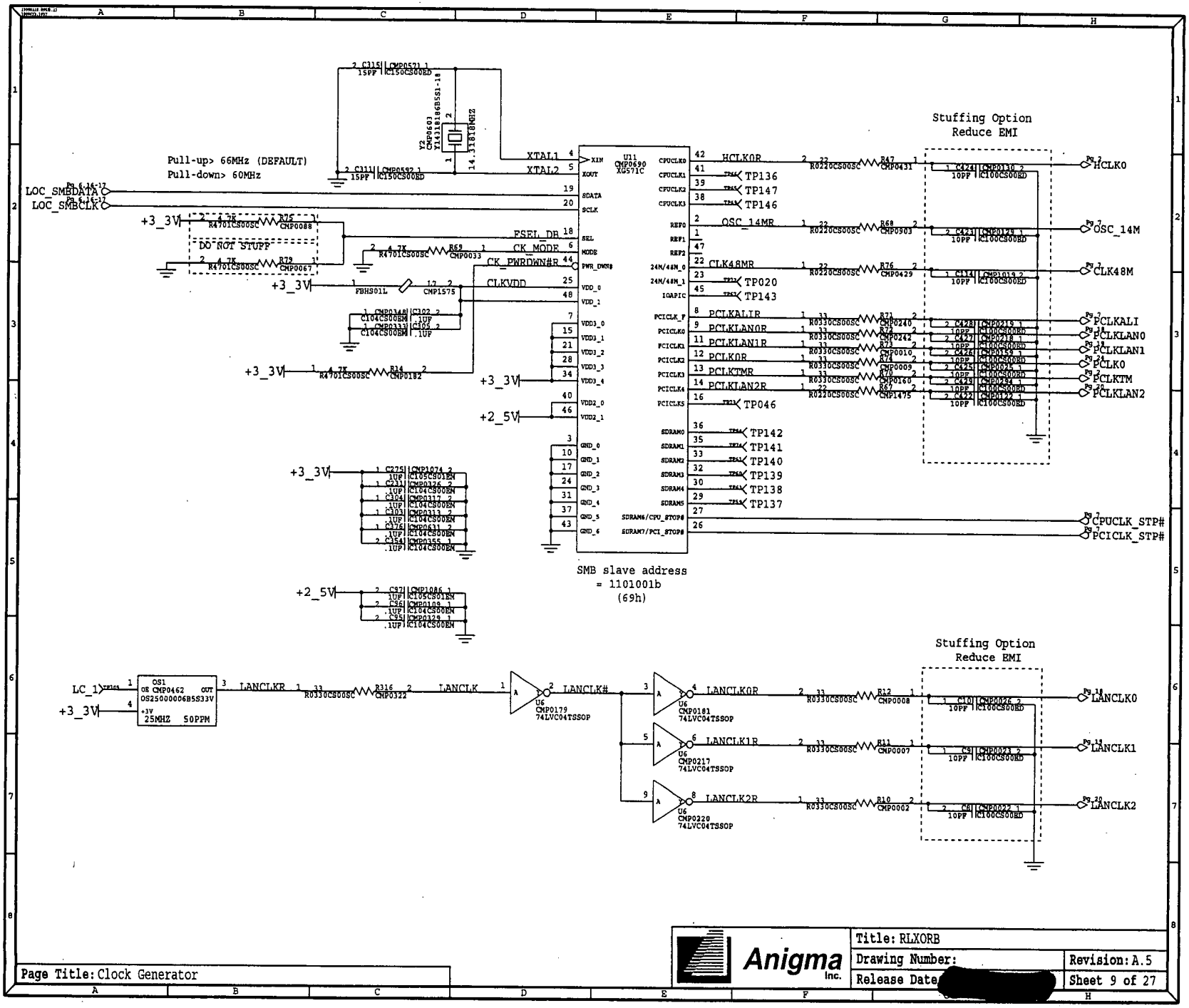
Title: RLXORB

Drawing Number:

Release Date [redacted]

Revision: A.5

Sheet 8 of 27



Page Title: Clock Generator

Anigma Inc.

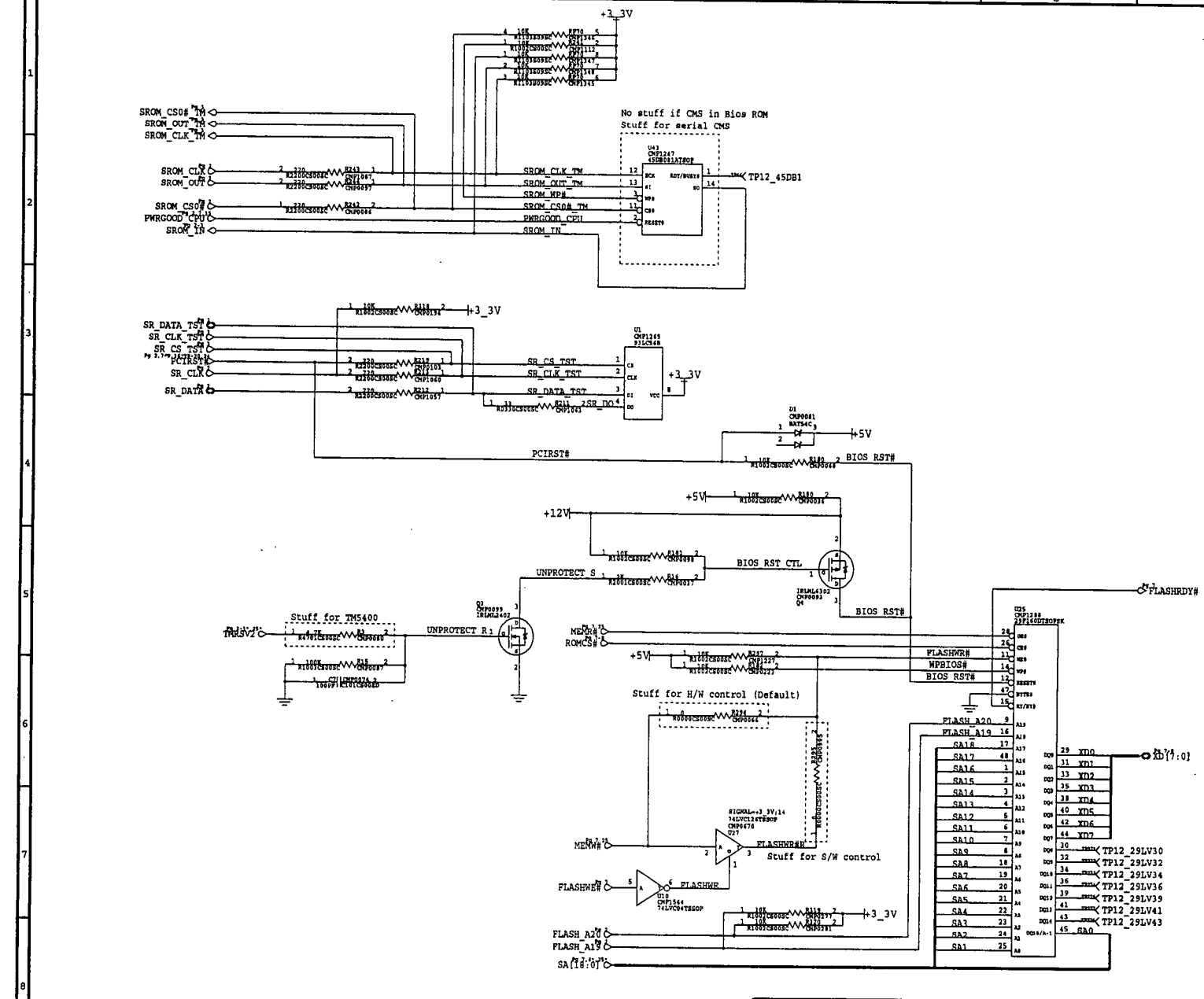
Title: RLXORB

Drawing Number:

Revision: A.5

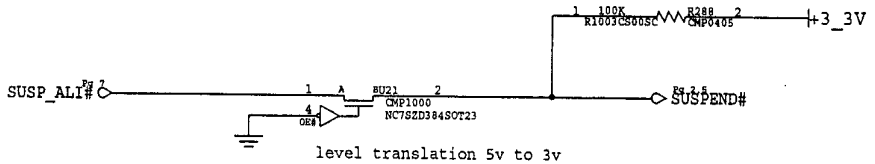
Release Date: [redacted]

Sheet 9 of 27



Anigma Inc.	Title: RLXORB	
	Drawing Number:	Revision: A.5
	Release Date: [redacted]	Sheet 10 of 27

Page Title: Flash/ID ROM



level translation 5v to 3v

Page Title: Suspend# Q-Switch

Anigma Inc.

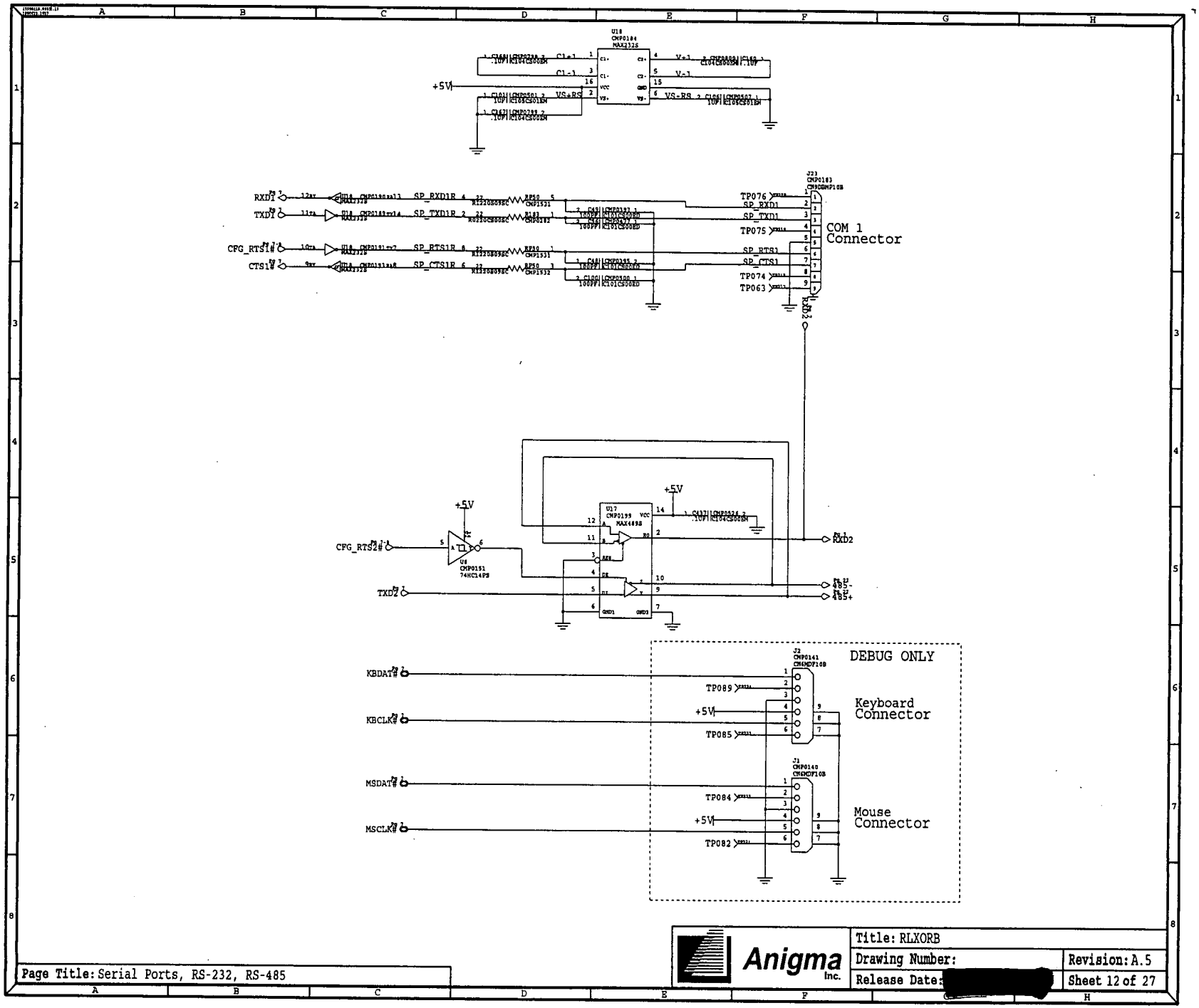
Title: RLXORB

Drawing Number:

Revision: A.5

Release Date: [redacted]

Sheet 11 of 27



Page Title: Serial Ports, RS-232, RS-485

Anigma Inc.

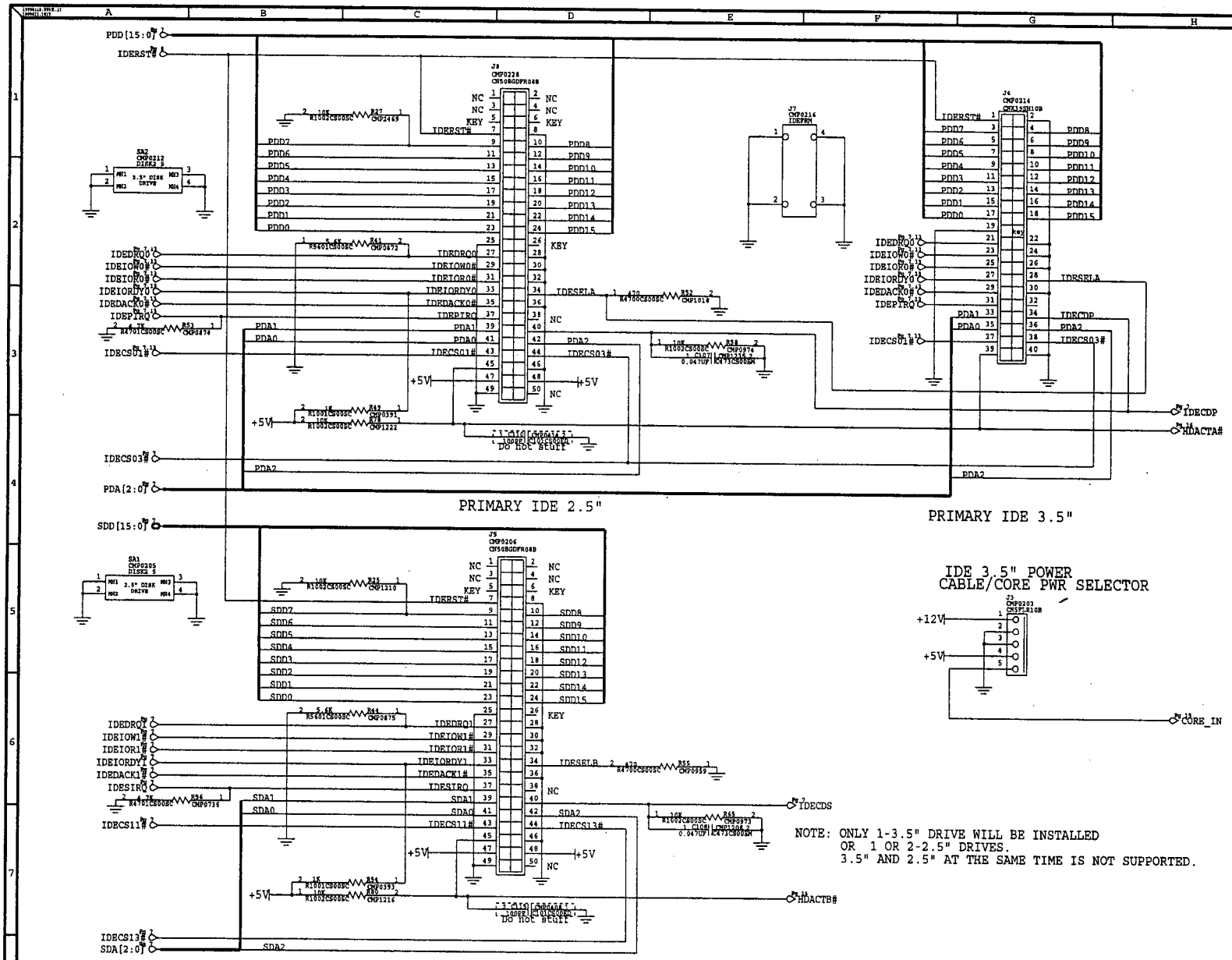
Title: RLXORB

Drawing Number:

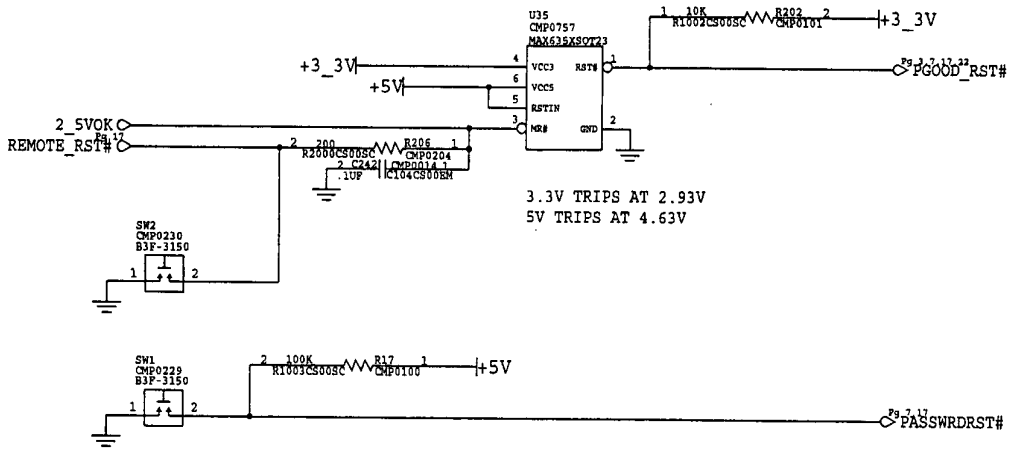
Revision: A.5

Release Date: [redacted]

Sheet 12 of 27



Page Title: IDE Interface	
Anigma Inc.	Title: RLXORB
	Drawing Number:
	Release Date: [redacted]
	Revision: A.5
	Sheet 13 of 27



Page Title: Voltage Monitoring / Reset control

Anigma Inc.

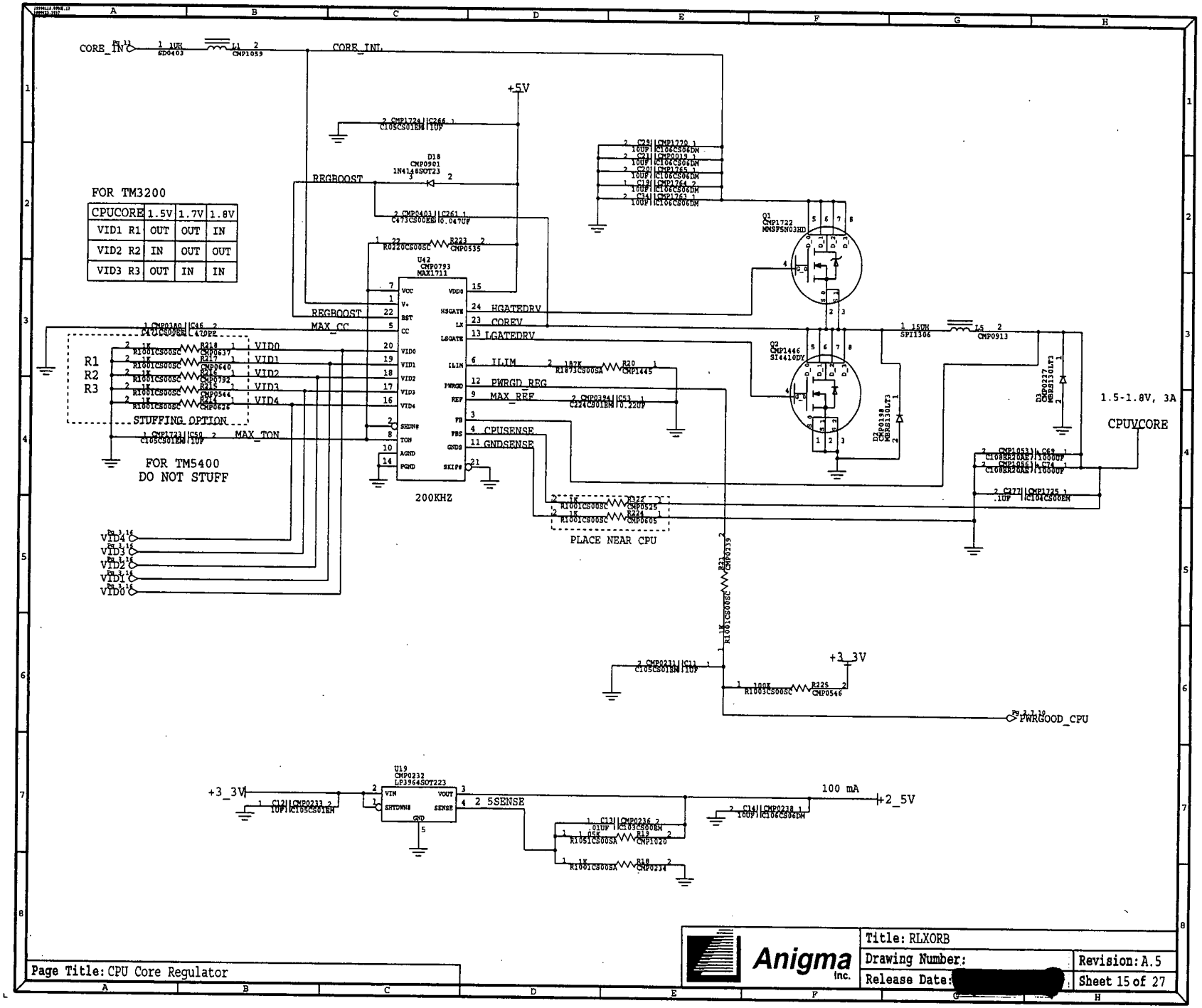
Title: RLXORB

Drawing Number:

Release Date: [redacted]

Revision: A.5

Sheet 14 of 27



Page Title: CPU Core Regulator

Anigma Inc.

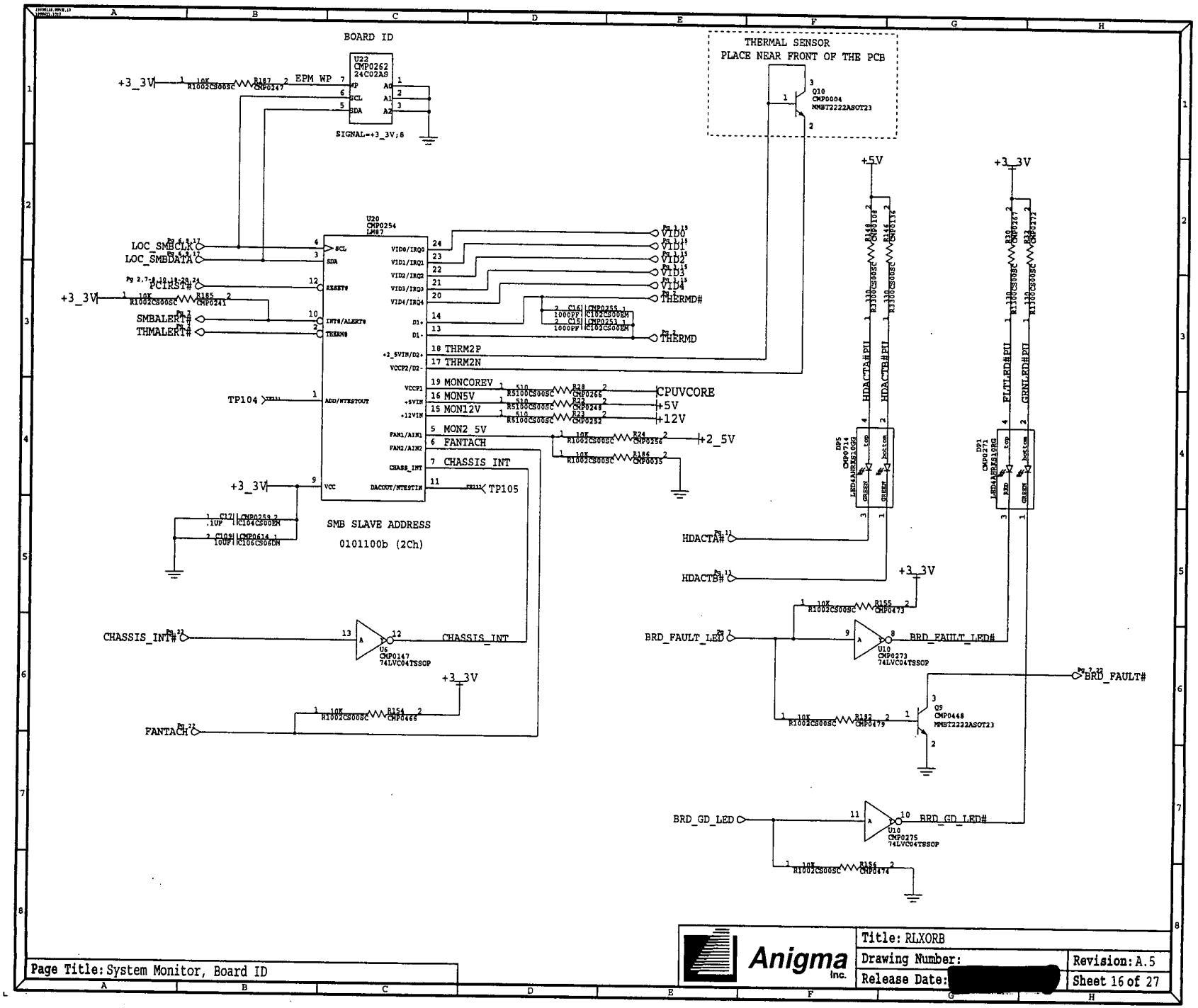
Title: RLXORB

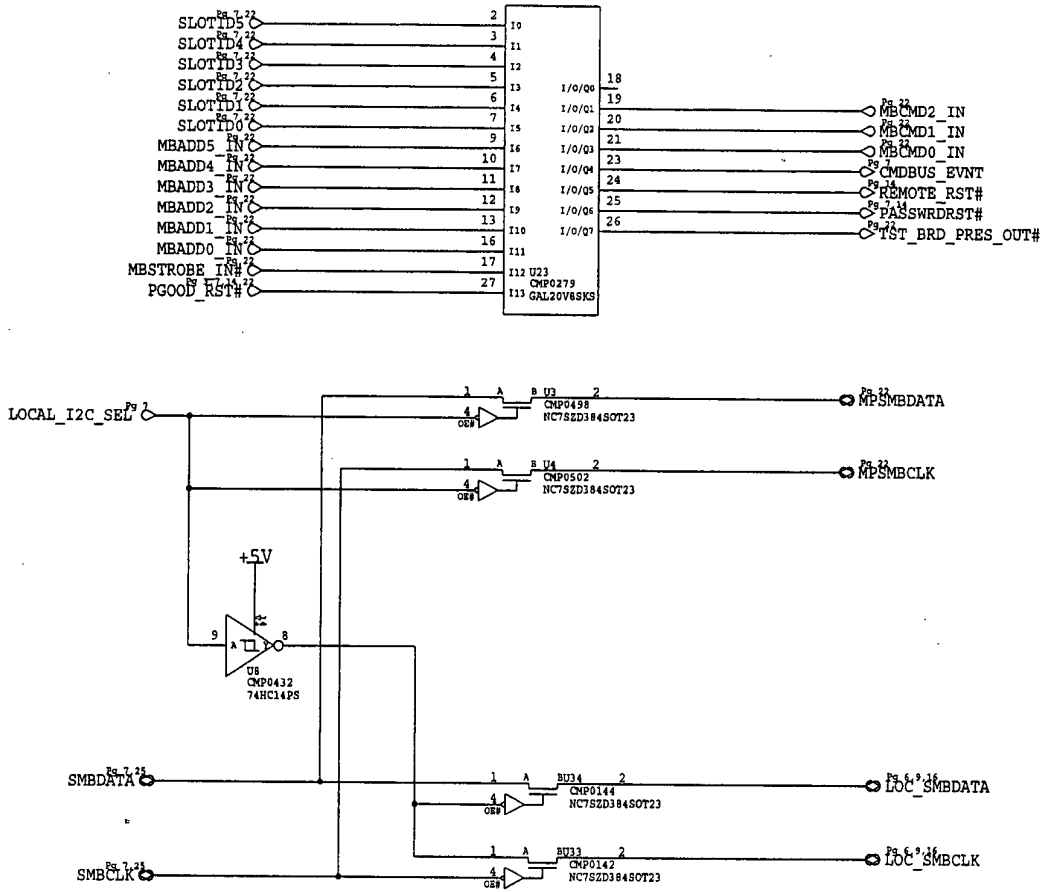
Drawing Number:

Release Date: [redacted]

Revision: A.5

Sheet 15 of 27


BOARD ID
U22
CMP0252
24C02AS
EPM WP
SIGNAL=+3_3V;8
THERMAL SENSOR
PLACE NEAR FRONT OF THE PCB
Q10
CMP0004
MMBT2222ASOT23
U20
CMP0254
LM87
LOC_SMBCLK
LOC_SMBDATA
PCIRST#
SMBALERT#
THMALERT#
VID0
VID1
VID2
VID3
VID4
THERMD#
THERMD
THRM2P
THRM2N
MONCOREV
MON5V
MON12V
MON2_5V
FANTACH
CHASSIS_INT
TP104
TP105
CPUVCORE
+5V
+12V
+2_5V
SMB SLAVE ADDRESS
0101100b (2Ch)
HDACTA#
HDACTB#
CHASSIS_INT#
FANTACH
BRD_FAULT_LED
BRD_FAULT_LED#
BRD_FAULT#
BRD_GD_LED
BRD_GD_LED#
Anigma
Inc.
Title: RLXORB
Drawing Number:
Release Date:
Revision: A.5
Sheet 16 of 27
Page Title: System Monitor, Board ID



Page Title: Management Logic

Anigma Inc.

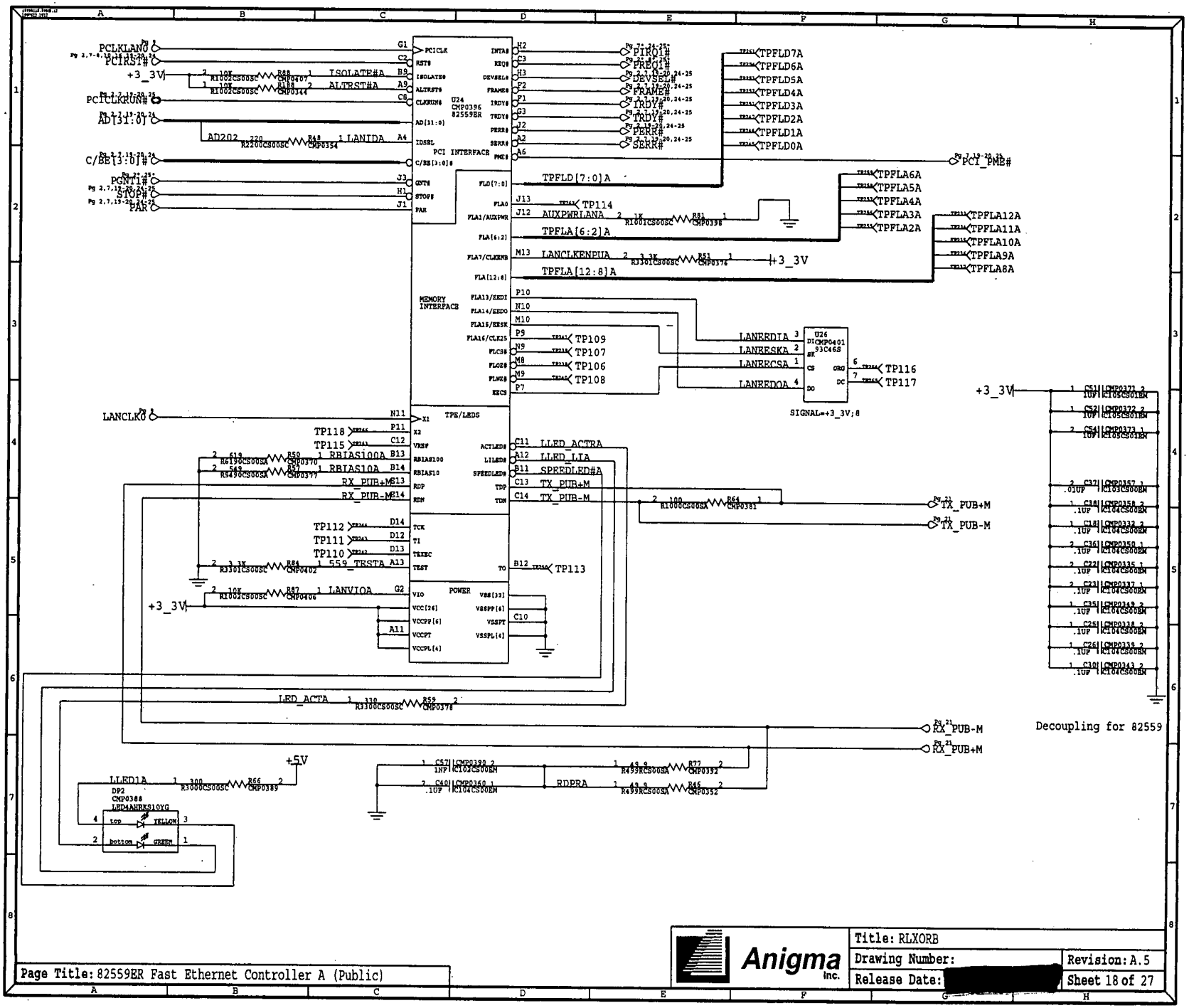
Title: RLXORB

Drawing Number:

Revision: A.5

Release Date: [redacted]

Sheet 17 of 27



Page Title: 82559ER Fast Ethernet Controller A (Public)

Anigma Inc.

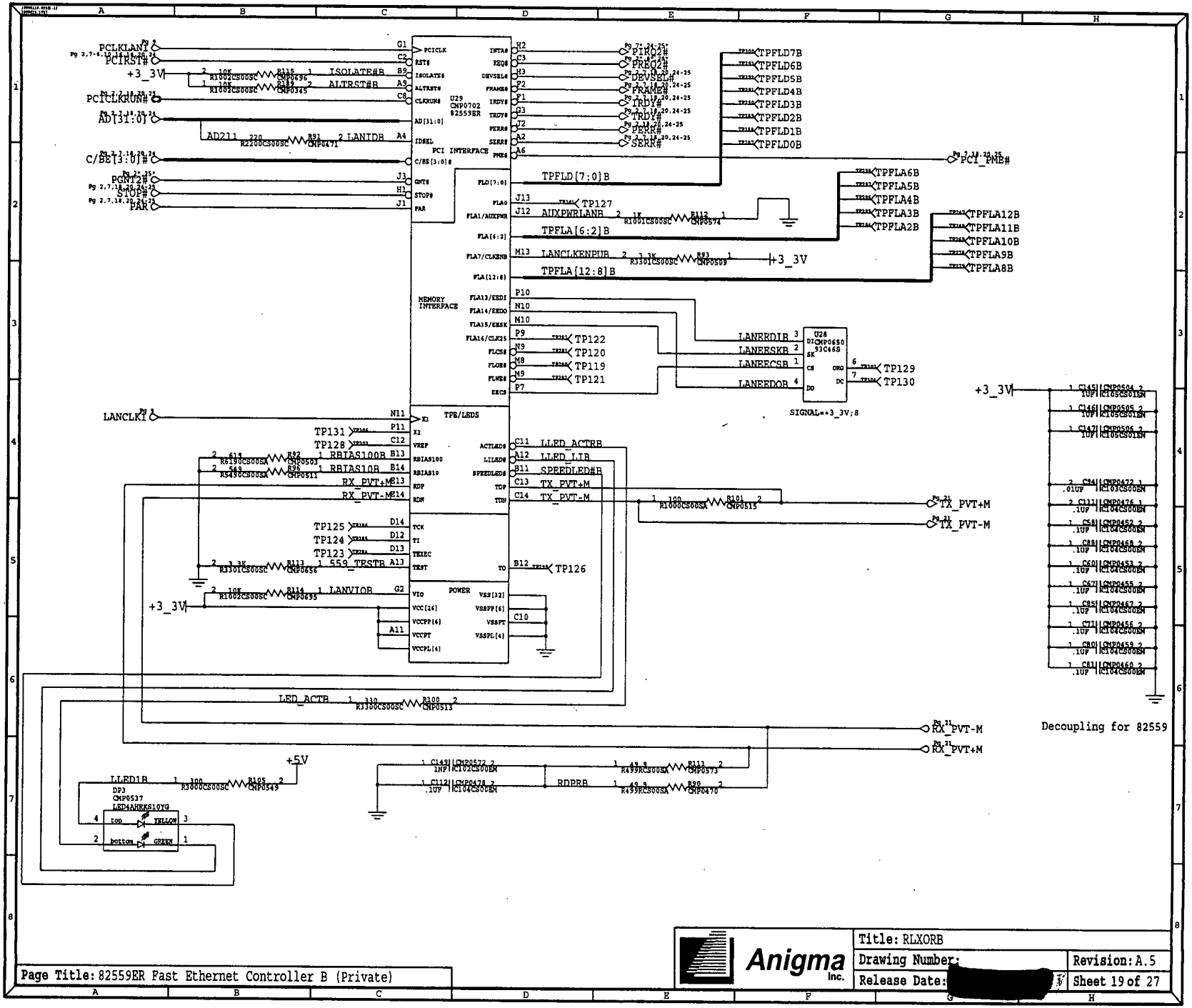
Title: RLXORB

Drawing Number:

Revision: A.5

Release Date: [redacted]

Sheet 18 of 27



Anigma Inc.

Title: RLXORB

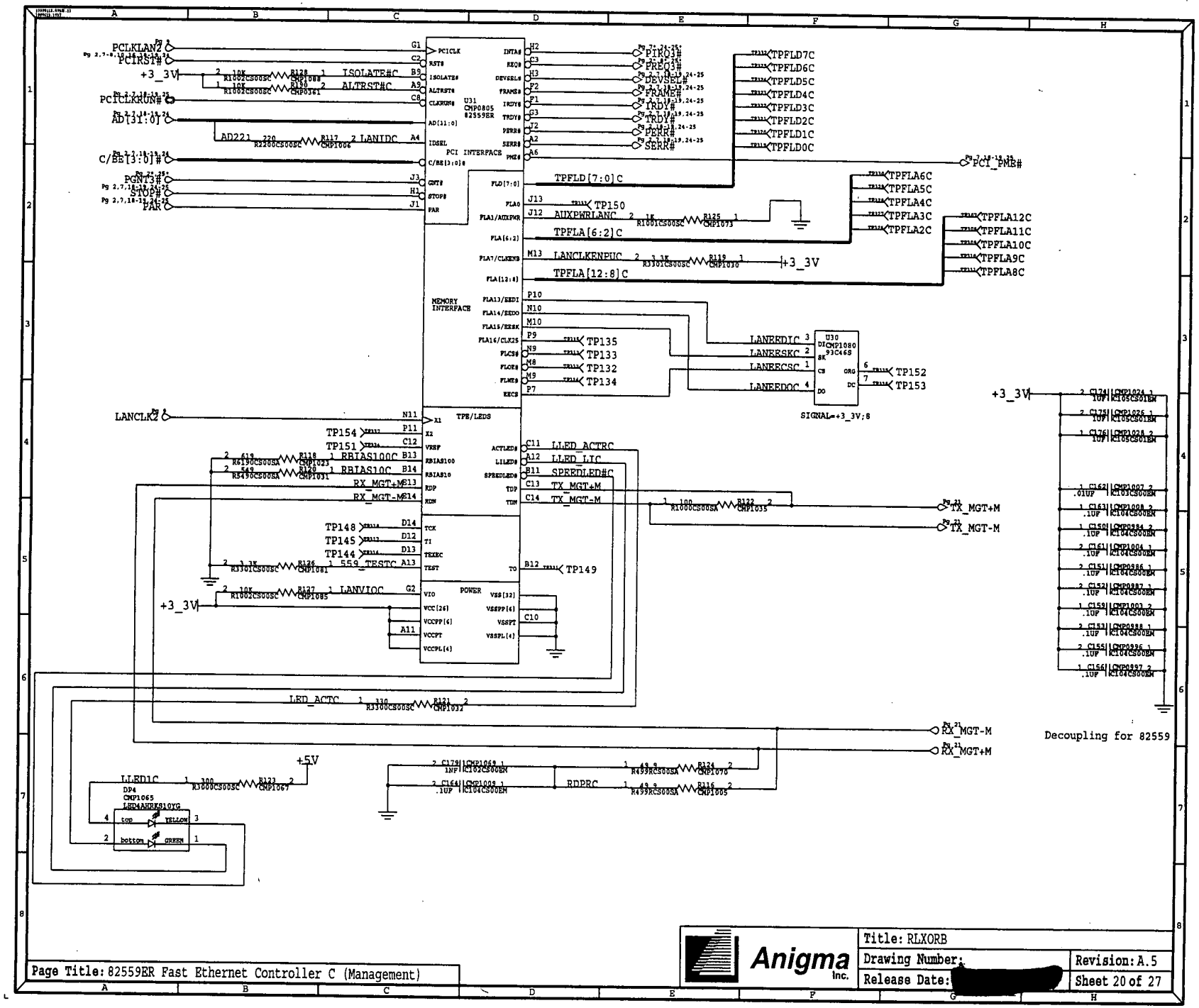
Drawing Number:

Revision: A.5

Release Date: [redacted]

Sheet 19 of 27

Page Title: 82559ER Fast Ethernet Controller B (Private)



Anigma Inc.

Title: RLXORB

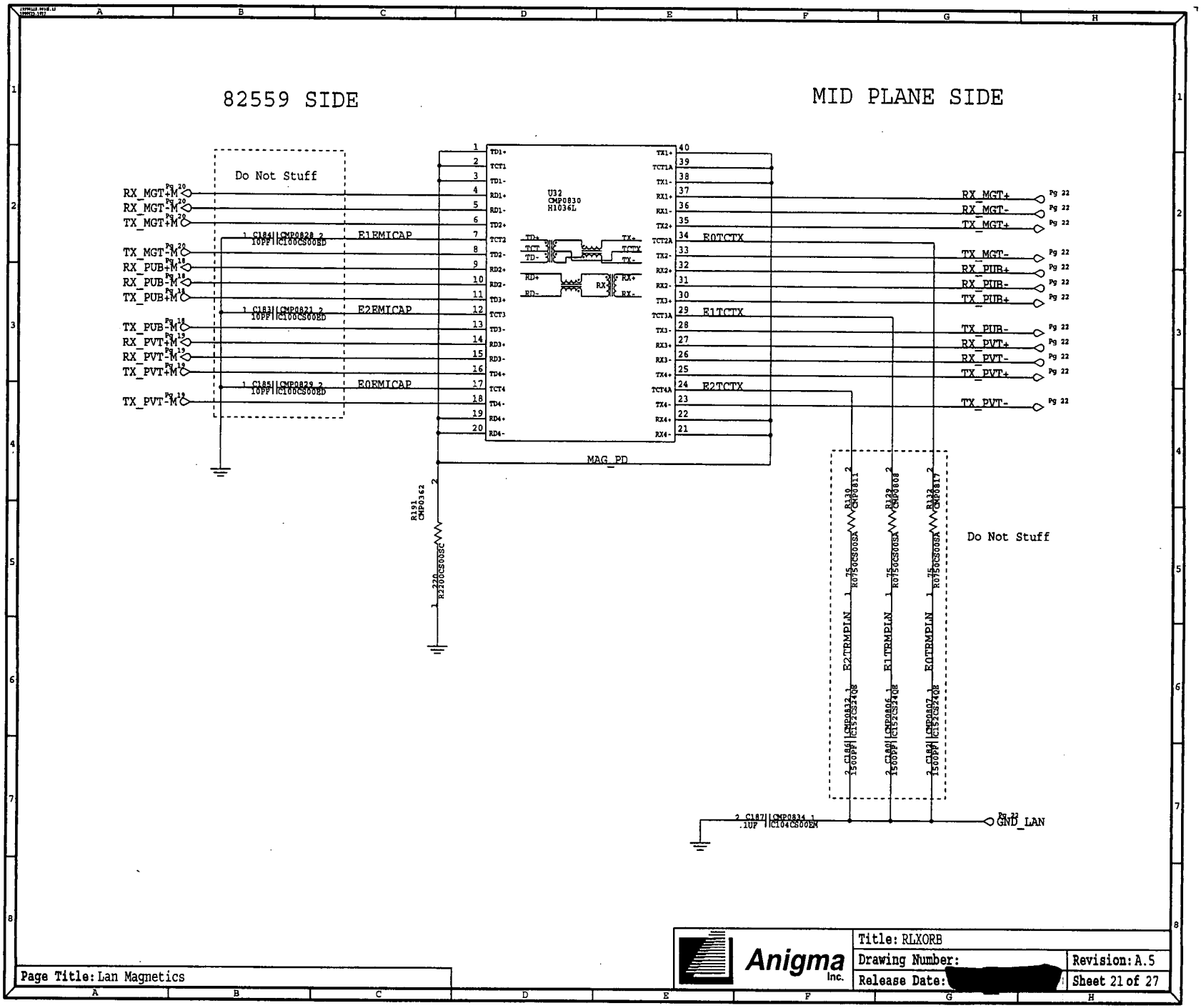
Drawing Number: [redacted]

Revision: A.5

Release Date: [redacted]

Sheet 20 of 27

Page Title: 82559ER Fast Ethernet Controller C (Management)



Page Title: Lan Magnetics

Anigma Inc.

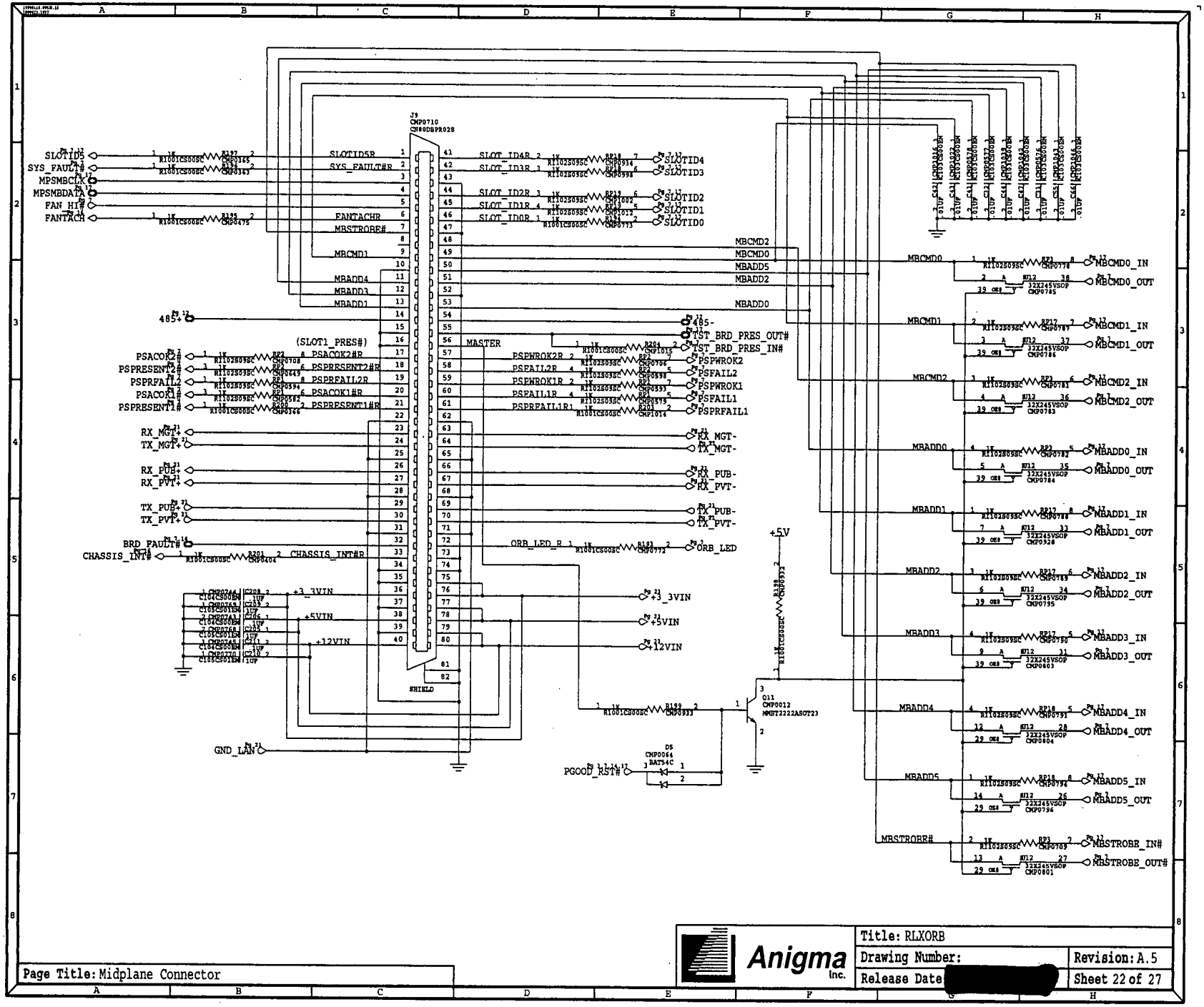
Title: RLXORB

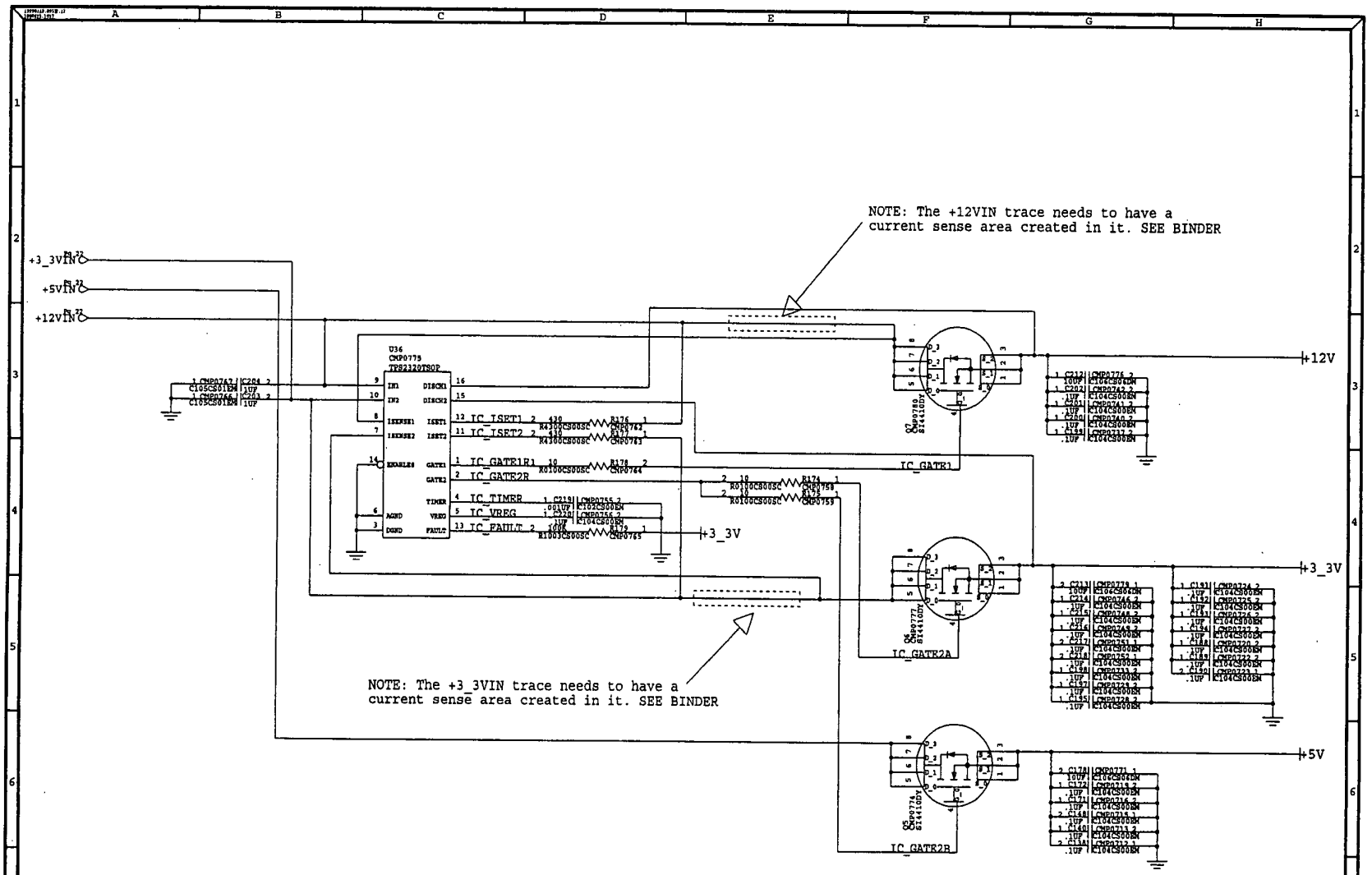
Drawing Number: [redacted]

Release Date: [redacted]

Revision: A.5

Sheet 21 of 27


SLOTID5
SYS_FAULT#
MPSMBCLK
MPSMBDATA
FAN_HI#
FANTACH
SLOTID5R
SYS_FAULT#R
FANTACHR
MBSTROBE#
MBCMD1
MBADD4
MBADD3
MBADD1
485+
485-
(SLOT1_PRES#)
PSACOK2#
PSPRESENT2#
PSPRFAIL2
PSACOK1#
PSPRESENT1#
PSACOK2#R
PSPRESENT2#R
PSPRFAIL2R
PSACOK1#R
PSPRESENT1#R
RX_MGT+
TX_MGT+
RX_PUB+
RX_PVT+
TX_PUB+
TX_PVT+
BRD_FAULT#
CHASSIS_INT#
CHASSIS_INT#R
+3_3VIN
+5VIN
+12VIN
GND_LAN
SHIELD
SLOT_ID4R
SLOT_ID3R
SLOT_ID2R
SLOT_ID1R
SLOT_ID0R
SLOTID4
SLOTID3
SLOTID2
SLOTID1
SLOTID0
MBCMD2
MBCMD0
MBADD5
MBADD2
MBADD0
MASTER
PSPWROK2R
PSFAIL2R
PSPWROK1R
PSFAIL1R
PSPRFAIL1R1
TST_BRD_PRES_OUT#
TST_BRD_PRES_IN#
PSPWROK2
PSFAIL2
PSPWROK1
PSFAIL1
PSPRFAIL1
RX_MGT-
TX_MGT-
RX_PUB-
RX_PVT-
TX_PUB-
TX_PVT-
ORB_LED_R
ORB_LED
+5V
Q11
CMP0012
MMST2222ASOT23
D5
CMP0064
BAT54C
PGOOD_RST#
MBCMD0_IN
MBCMD0_OUT
MBCMD1_IN
MBCMD1_OUT
MBCMD2_IN
MBCMD2_OUT
MBADD0_IN
MBADD0_OUT
MBADD1_IN
MBADD1_OUT
MBADD2_IN
MBADD2_OUT
MBADD3_IN
MBADD3_OUT
MBADD4_IN
MBADD4_OUT
MBADD5_IN
MBADD5_OUT
MBSTROBE_IN#
MBSTROBE_OUT#
Anigma Inc.
Title: RLXORB
Drawing Number:
Revision: A.5
Release Date
Sheet 22 of 27
Page Title: Midplane Connector



Page Title: Inrush Current Control

Anigma Inc.

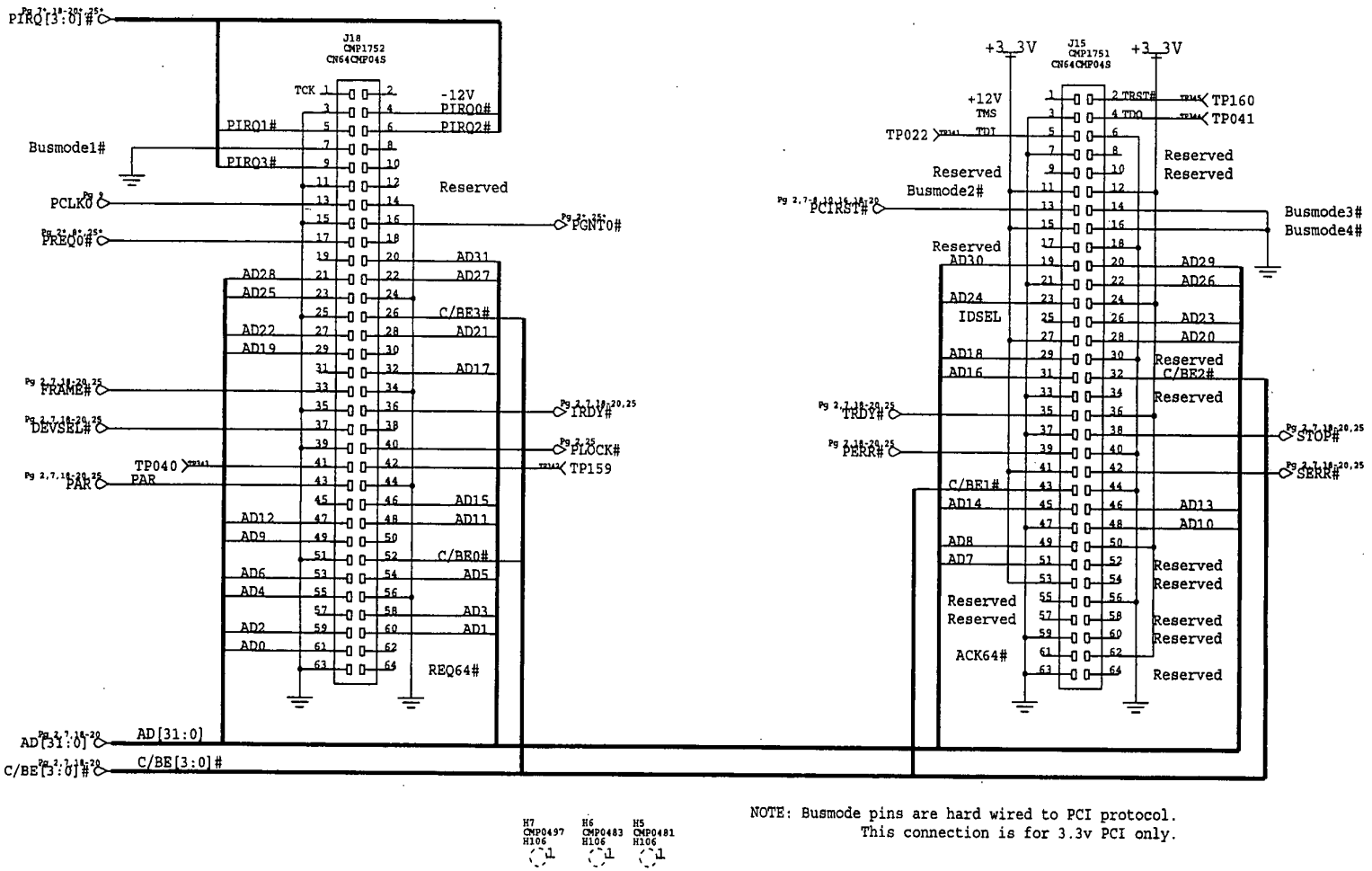
Title: RLXORB

Drawing Number:

Revision: A.5

Release Date [redacted]

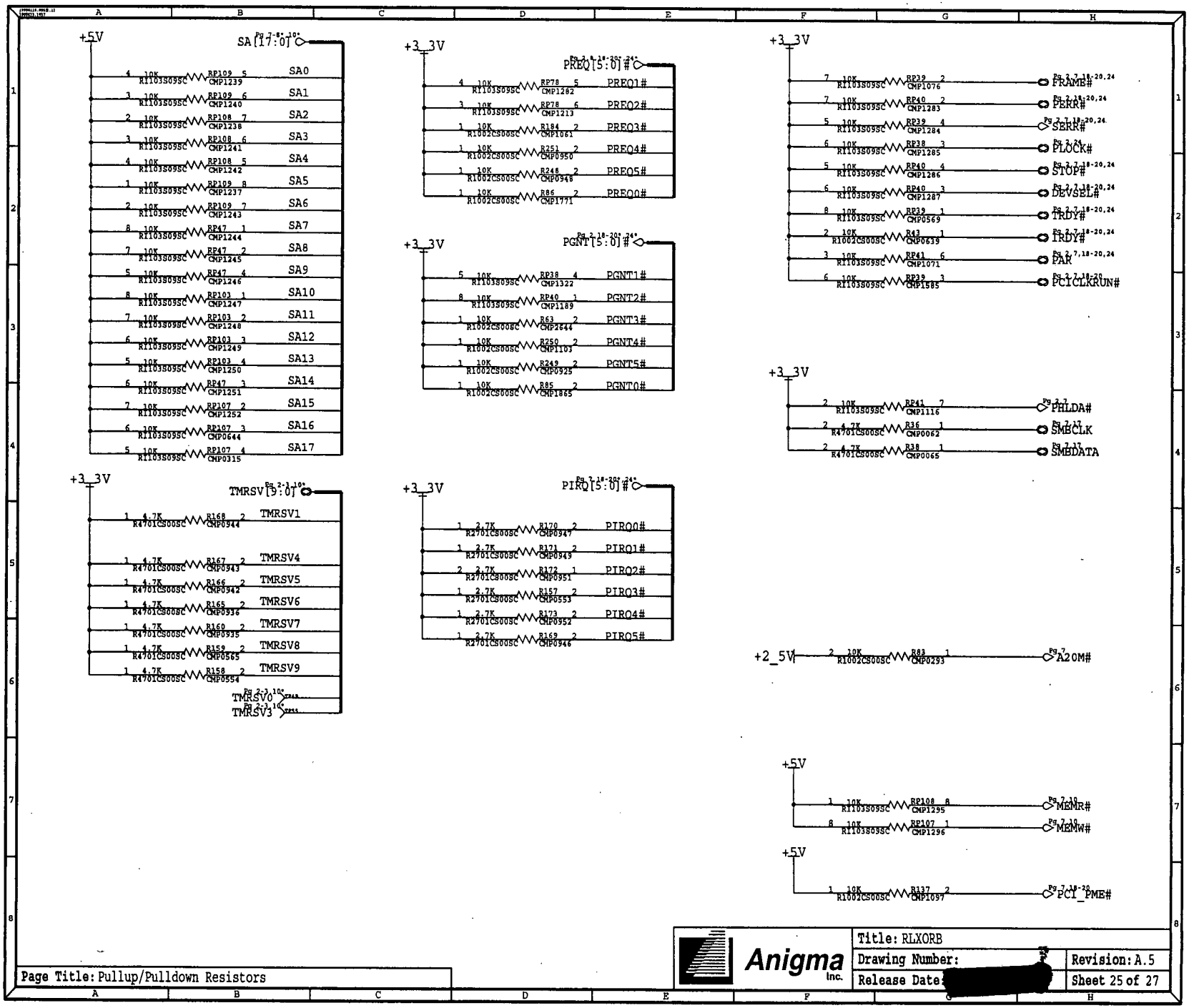
Sheet 23 of 27



NOTE: Busmode pins are hard wired to PCI protocol.
This connection is for 3.3v PCI only.

PMC CONNECTORS

Page Title: PMC Debug Connectors	Anigma Inc.	Title: RLXORB
		Drawing Number: [redacted]
		Release Date [redacted]
		Revision: A.5
		Sheet 24 of 27



Page Title: Pullup/Pulldown Resistors

Anigma Inc.

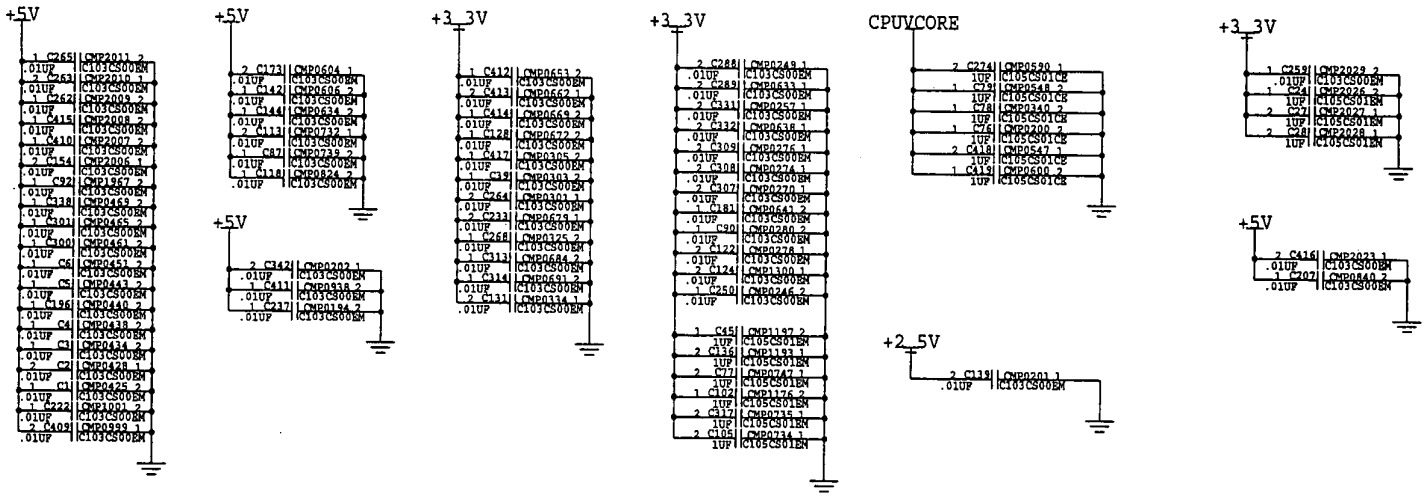
Title: RLXORB

Drawing Number: [redacted]

Release Date: [redacted]

Revision: A.5

Sheet 25 of 27



Page Title: Decoupling Capacitors

Anigma Inc.

Title: RLXORB

Drawing Number: [redacted]

Revision: A.5

Release Date: [redacted]

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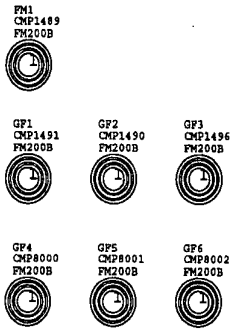
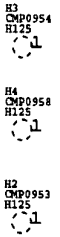
Ejector Hole

Fiducial Marks



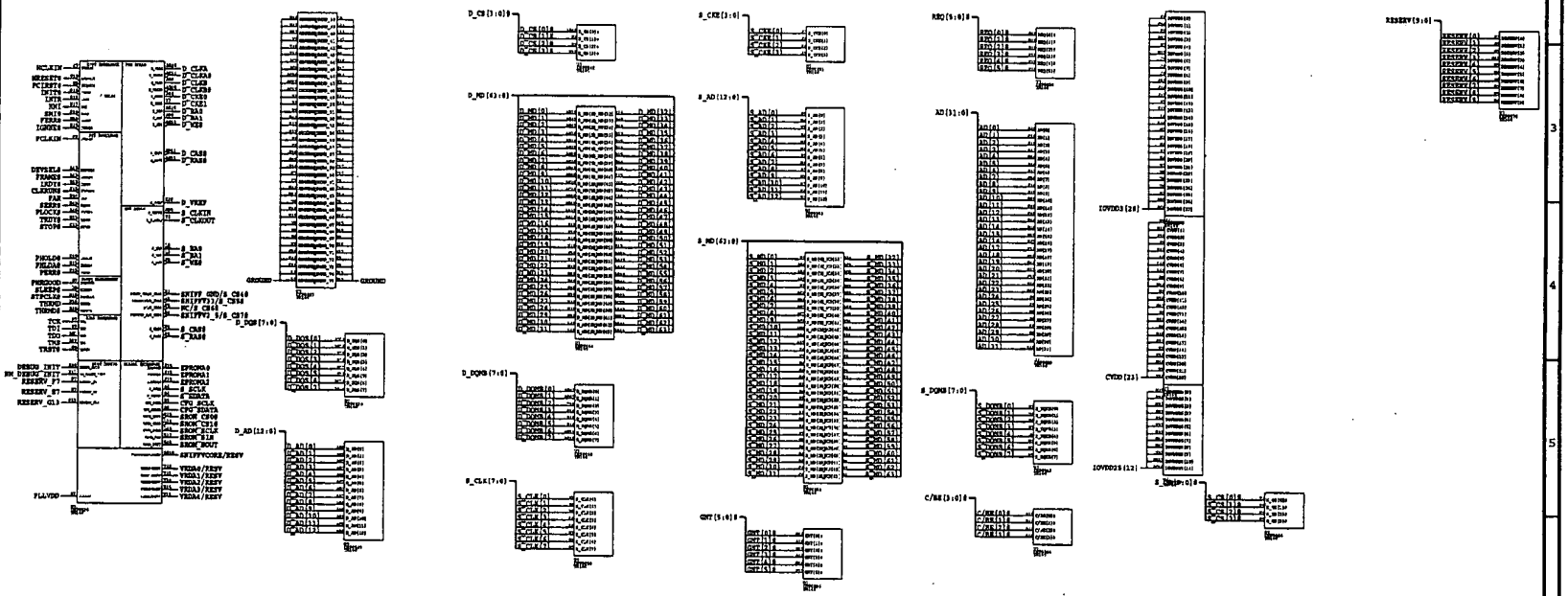
Tooling Holes



Page Title: Fiducials, Holes, Spare Gates

Anigma Inc.

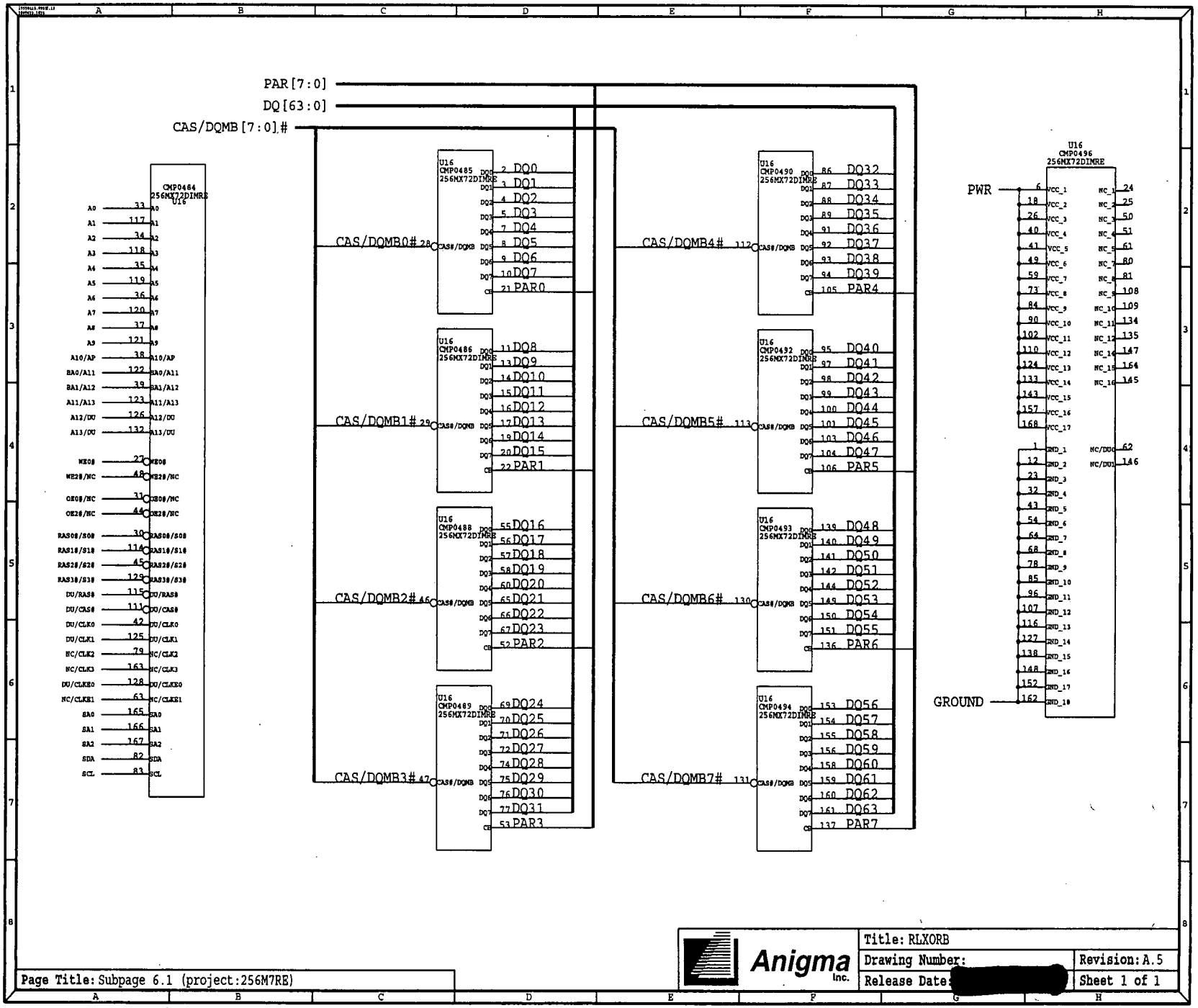
Title: RLXORB	
Drawing Number:	Revision: A.5
Release Date: [redacted]	Sheet 27 of 27

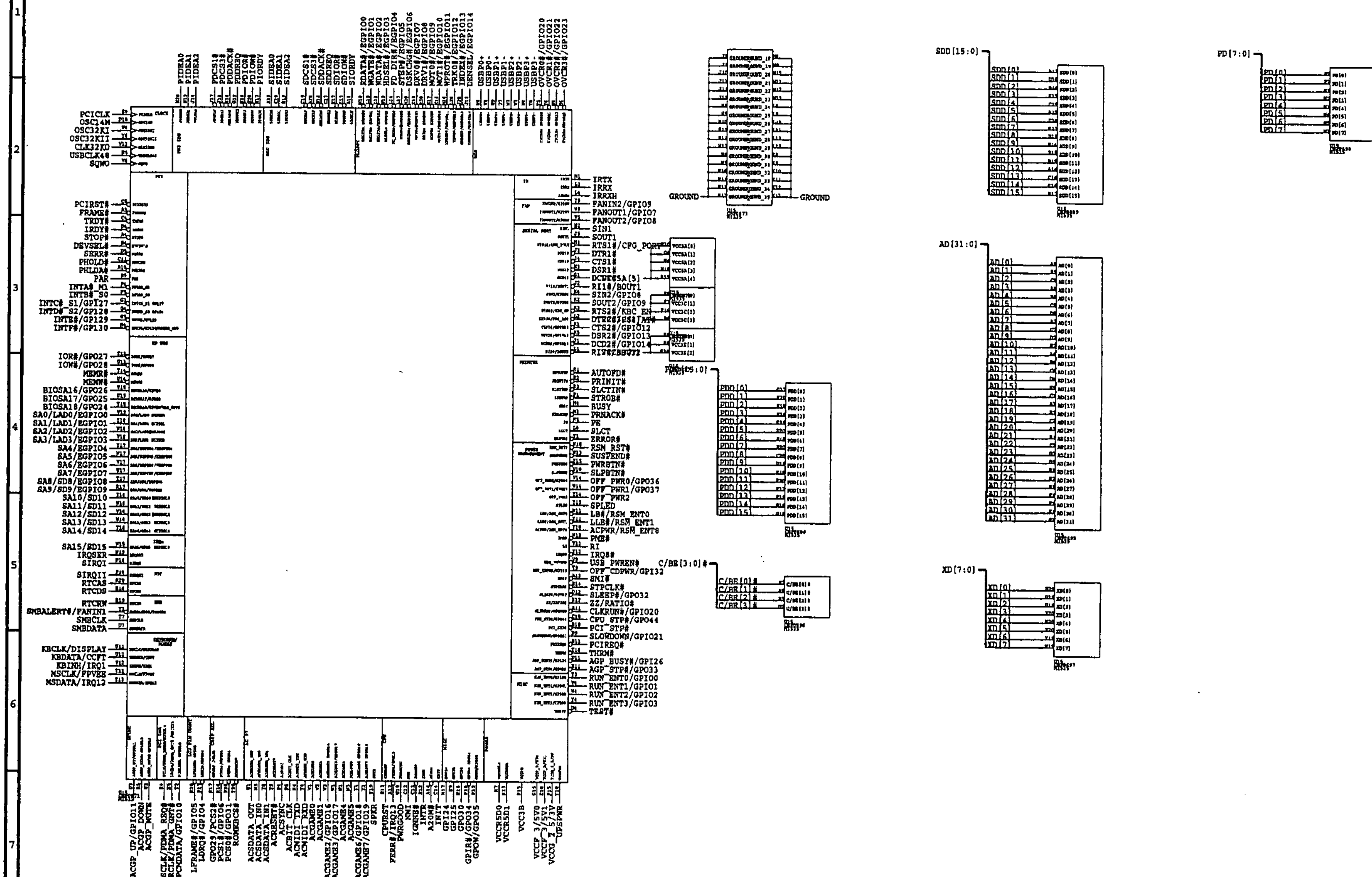


Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.5
Release Date [redacted]	Sheet 1 of 1

Page Title: Subpage 2.1 (project:TM160)


PAR[7:0]
DQ[63:0]
CAS/DQMB[7:0]#
CAS/DQMB0#
CAS/DQMB1#
CAS/DQMB2#
CAS/DQMB3#
CAS/DQMB4#
CAS/DQMB5#
CAS/DQMB6#
CAS/DQMB7#
PWR
GROUND
Anigma Inc.
Title: RLXORB
Drawing Number:
Release Date:
Revision: A.5
Sheet 1 of 1
Page Title: Subpage 6.1 (project:256M7RE)



Page Title: Subpage 7.1 (project:M1535)

Anigma Inc.

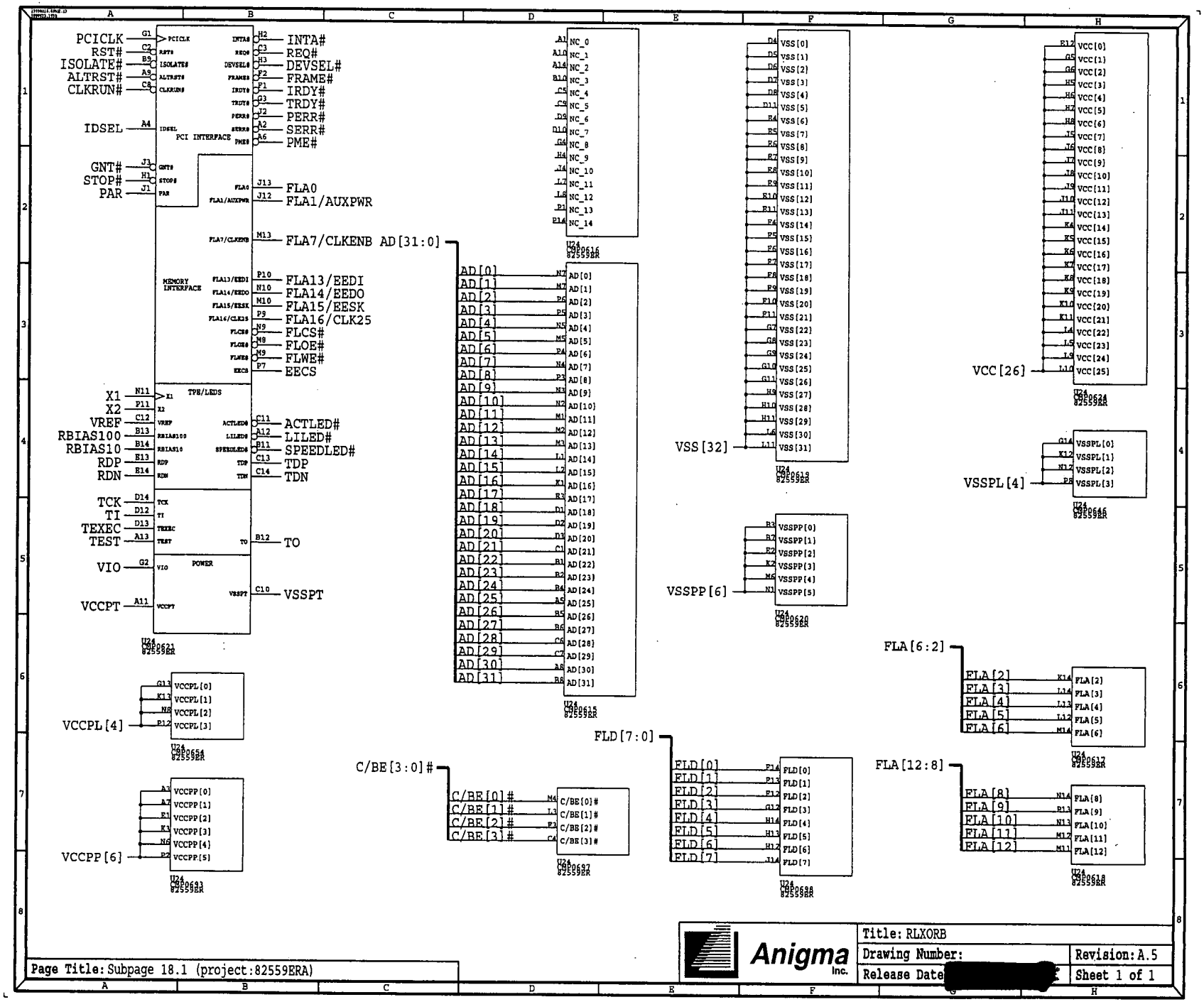
Title: RLXORB

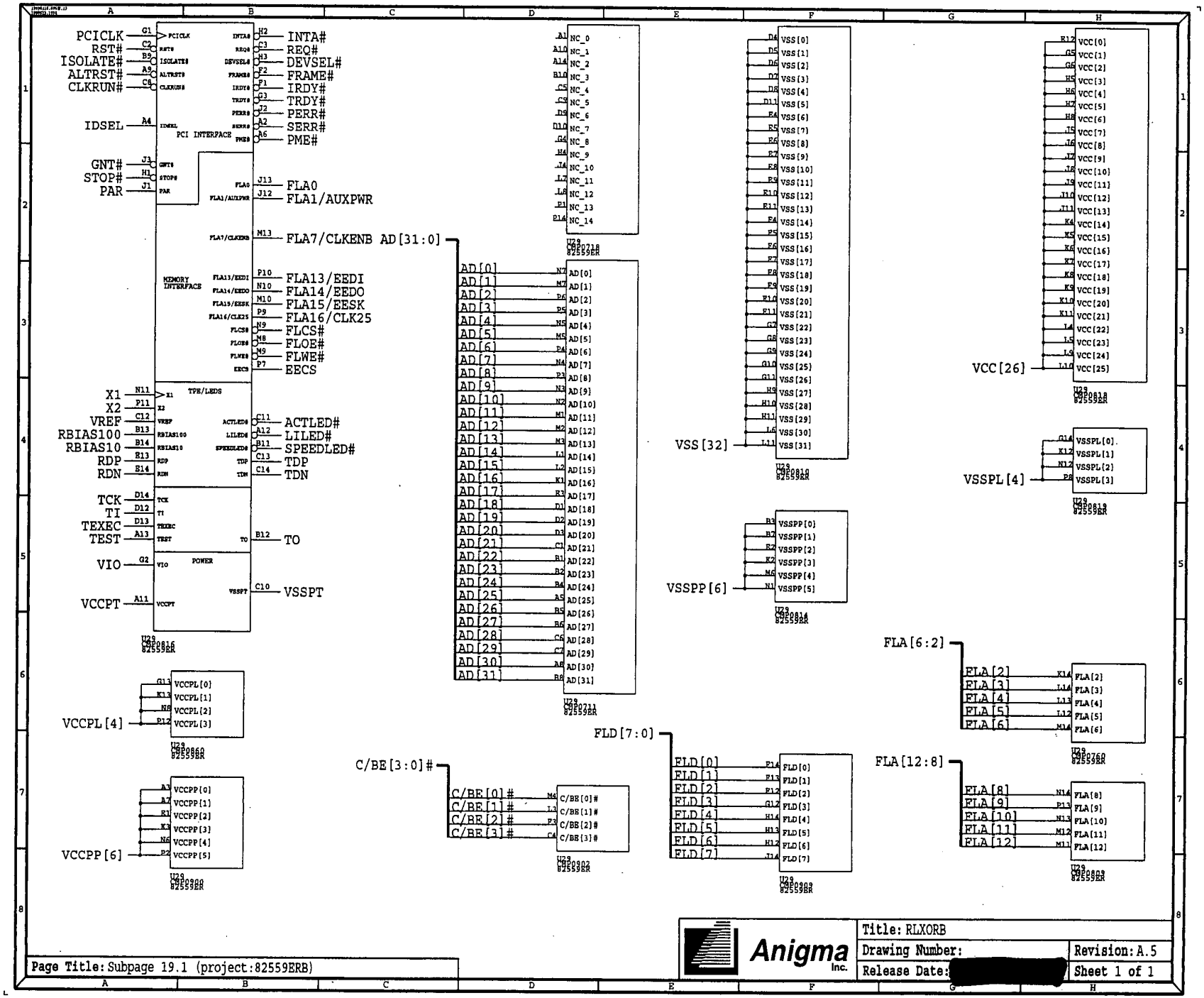
Drawing Number:

Release Date [redacted]

Revision: A.5

Sheet 1 of 1


PCICLK
RST#
ISOLATE#
ALTRST#
CLKRUN#
IDSEL
PCI INTERFACE
INTA#
REQ#
DEVSEL#
FRAME#
IRDY#
TRDY#
PERR#
SERR#
PME#
GNT#
STOP#
PAR
FLA0
FLA1/AUXPWR
FLA7/CLKENB
MEMORY INTERFACE
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16/CLK25
FLCS#
FLOE#
FLWE#
EECS
TPE/LEDS
X1
X2
VREF
RBIAS100
RBIAS10
RDP
RDN
ACTLED#
LILED#
SPEEDLED#
TDP
TDN
TCK
TI
TEXEC
TEST
TO
POWER
VIO
VCCPT
VSSPT
AD[31:0]
VCCPL[4]
VCCPP[6]
C/BE[3:0]#
FLD[7:0]
VSS[32]
VSSPP[6]
VCC[26]
VSSPL[4]
FLA[6:2]
FLA[12:8]
Anigma Inc.
Title: RLXORB
Drawing Number:
Revision: A.5
Release Date
Sheet 1 of 1
Page Title: Subpage 18.1 (project:82559ERA)


PCICLK
RST#
ISOLATE#
ALTRST#
CLKRUN#
IDSEL
GNT#
STOP#
PAR
PCI INTERFACE
INTA#
REQ#
DEVSEL#
FRAME#
IRDY#
TRDY#
PERR#
SERR#
PME#
FLA0
FLA1/AUXPWR
FLA7/CLKENB
MEMORY INTERFACE
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16/CLK25
FLCS#
FLOE#
FLWE#
EECS
TPE/LEDS
X1
X2
VREF
RBIAS100
RBIAS10
RDP
RDN
ACTLED#
LILED#
SPEEDLED#
TDP
TDN
TCK
TI
TEXEC
TEST
TO
POWER
VIO
VCCPT
VSSPT
VCCPL[4]
VCCPP[6]
AD[31:0]
C/BE[3:0]#
FLD[7:0]
VSS[32]
VSSPP[6]
VCC[26]
VSSPL[4]
FLA[6:2]
FLA[12:8]
Anigma Inc.
Title: RLXORB
Drawing Number:
Revision: A.5
Release Date:
Sheet 1 of 1
Page Title: Subpage 19.1 (project:82559ERB)

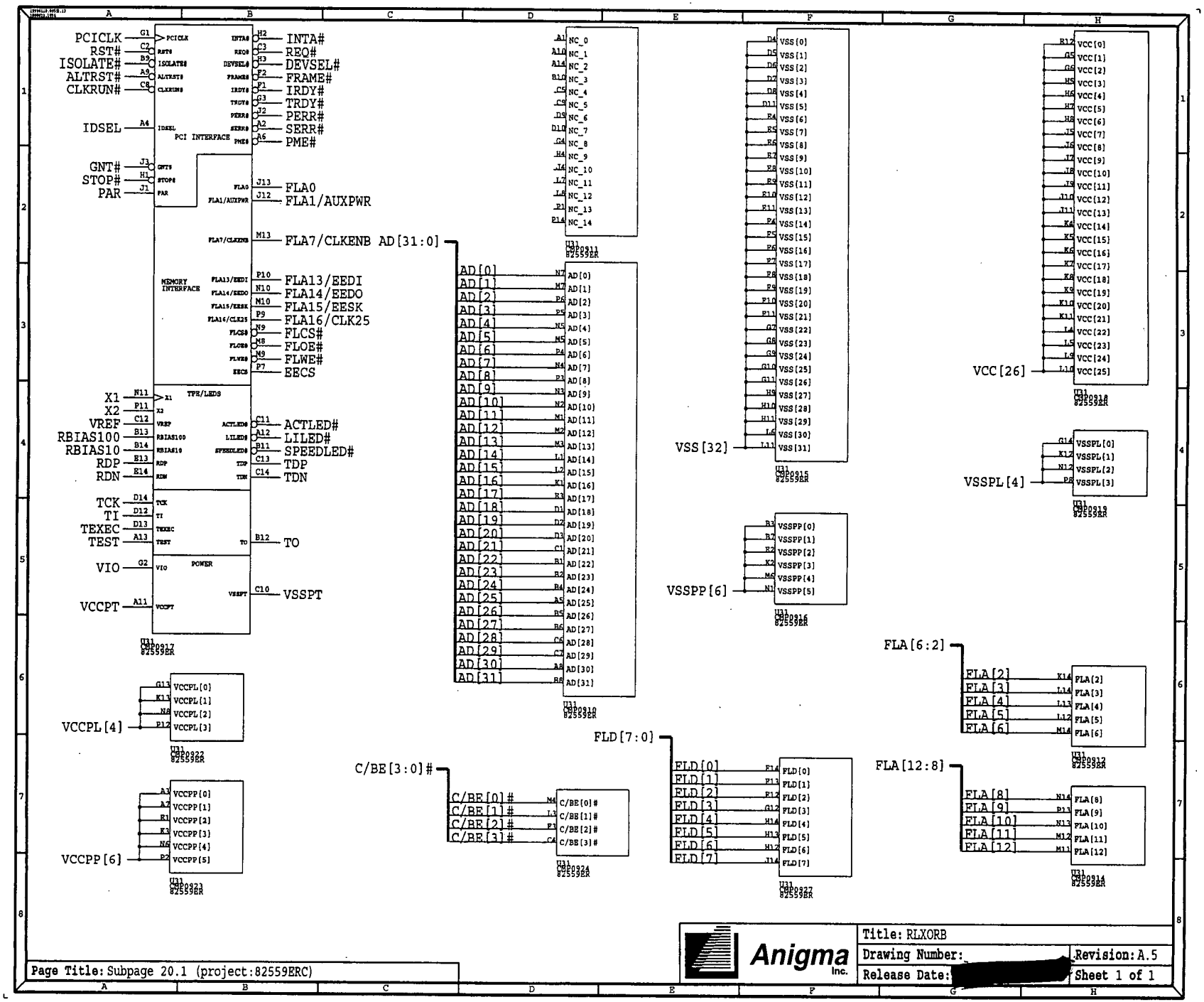

PCICLK
RST#
ISOLATE#
ALTRST#
CLKRUN#
IDSEL
GNT#
STOP#
PAR
INTA#
REQ#
DEVSEL#
FRAME#
IRDY#
TRDY#
PERR#
SERR#
PME#
PCI INTERFACE
FLA0
FLA1/AUXPWR
FLA7/CLKENB
MEMORY INTERFACE
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16/CLK25
FLCS#
FLOE#
FLWE#
EECS
X1
X2
VREF
RBIAS100
RBIAS10
RDP
RDN
TPR/LEDS
ACTLED#
LILED#
SPEEDLED#
TDP
TDN
TCK
TI
TEXEC
TEST
TO
VIO
VCCPT
POWER
VSSPT
AD[31:0]
NC_0
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
VSS[32]
VSS[0]
VSS[1]
VSS[2]
VSS[3]
VSS[4]
VSS[5]
VSS[6]
VSS[7]
VSS[8]
VSS[9]
VSS[10]
VSS[11]
VSS[12]
VSS[13]
VSS[14]
VSS[15]
VSS[16]
VSS[17]
VSS[18]
VSS[19]
VSS[20]
VSS[21]
VSS[22]
VSS[23]
VSS[24]
VSS[25]
VSS[26]
VSS[27]
VSS[28]
VSS[29]
VSS[30]
VSS[31]
VCC[26]
VCC[0]
VCC[1]
VCC[2]
VCC[3]
VCC[4]
VCC[5]
VCC[6]
VCC[7]
VCC[8]
VCC[9]
VCC[10]
VCC[11]
VCC[12]
VCC[13]
VCC[14]
VCC[15]
VCC[16]
VCC[17]
VCC[18]
VCC[19]
VCC[20]
VCC[21]
VCC[22]
VCC[23]
VCC[24]
VCC[25]
VSSPL[4]
VSSPL[0]
VSSPL[1]
VSSPL[2]
VSSPL[3]
VSSPP[6]
VSSPP[0]
VSSPP[1]
VSSPP[2]
VSSPP[3]
VSSPP[4]
VSSPP[5]
VCCPL[4]
VCCPL[0]
VCCPL[1]
VCCPL[2]
VCCPL[3]
VCCPP[6]
VCCPP[0]
VCCPP[1]
VCCPP[2]
VCCPP[3]
VCCPP[4]
VCCPP[5]
C/BE[3:0]#
C/BE[0]#
C/BE[1]#
C/BE[2]#
C/BE[3]#
FLD[7:0]
FLD[0]
FLD[1]
FLD[2]
FLD[3]
FLD[4]
FLD[5]
FLD[6]
FLD[7]
FLA[6:2]
FLA[2]
FLA[3]
FLA[4]
FLA[5]
FLA[6]
FLA[12:8]
FLA[8]
FLA[9]
FLA[10]
FLA[11]
FLA[12]
Anigma Inc.
Title: RLXORB
Drawing Number:
Revision: A.5
Release Date:
Sheet 1 of 1
Page Title: Subpage 20.1 (project:82559ERC)

EXHIBIT C

Released Rev. A.6 (000628.1650)

Page Title: Index

Anigma Inc.

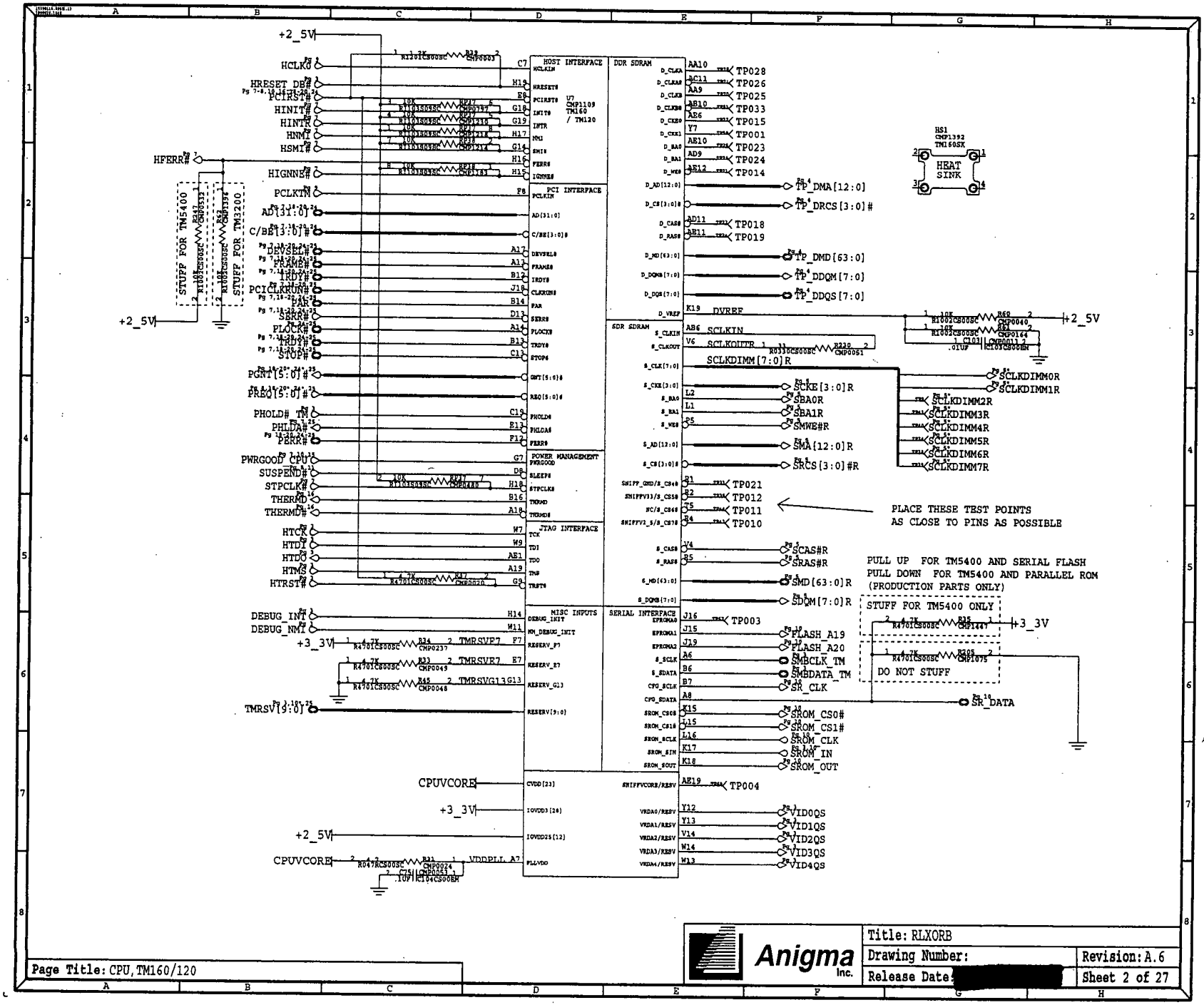
Title: RLXORB

Drawing Number:

Release Date [redacted]

Revision: A.6

Sheet 1 of 27



Page Title: CPU, TM160/120

Anigma Inc.

Title: RLXORB

Drawing Number:

Release Date: [redacted]

Revision: A.6

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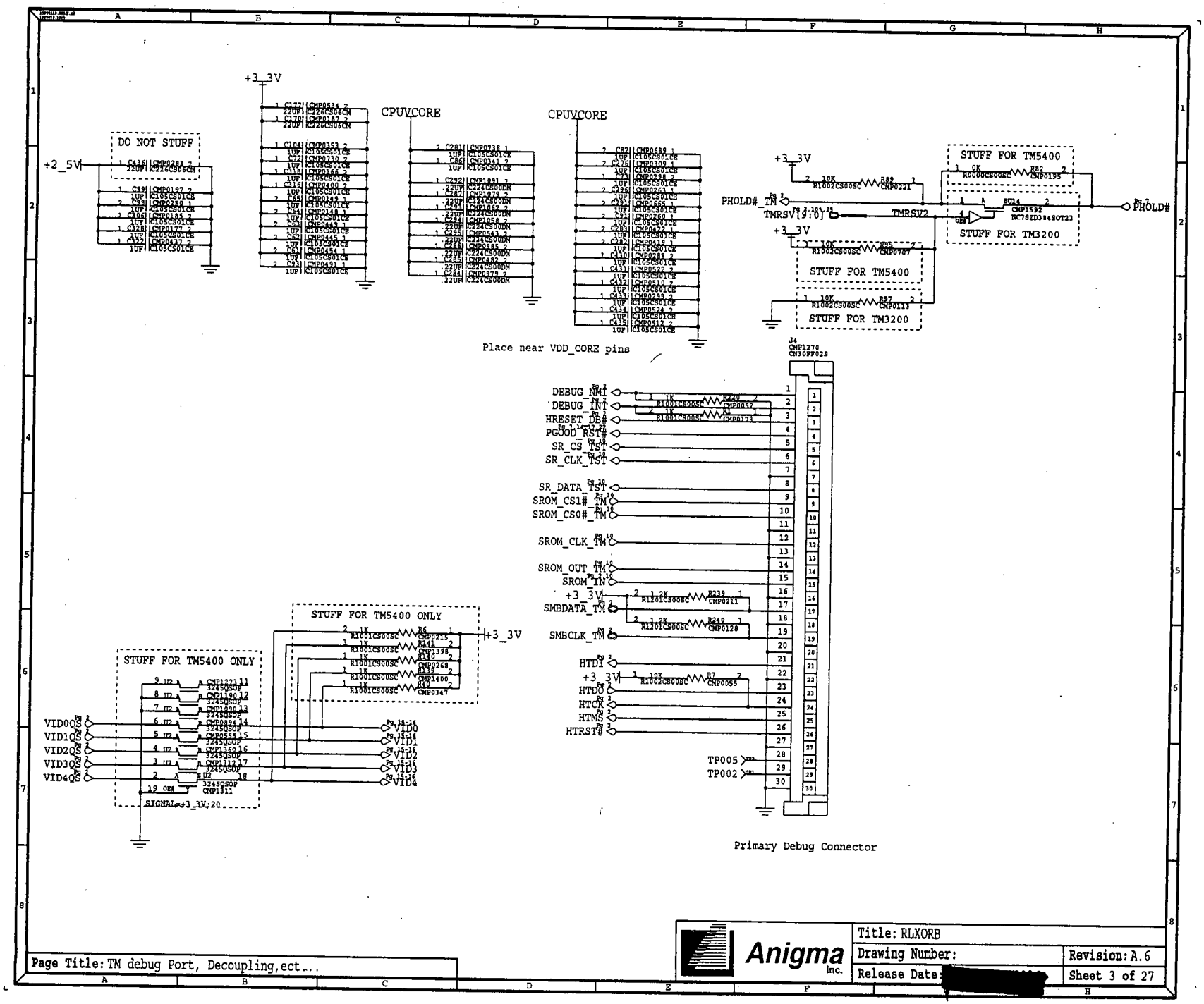

Page Title: TM debug Port, Decoupling,ect...

Anigma Inc.

Title: RLXORB

Drawing Number:

Revision: A.6

Release Date: [redacted]

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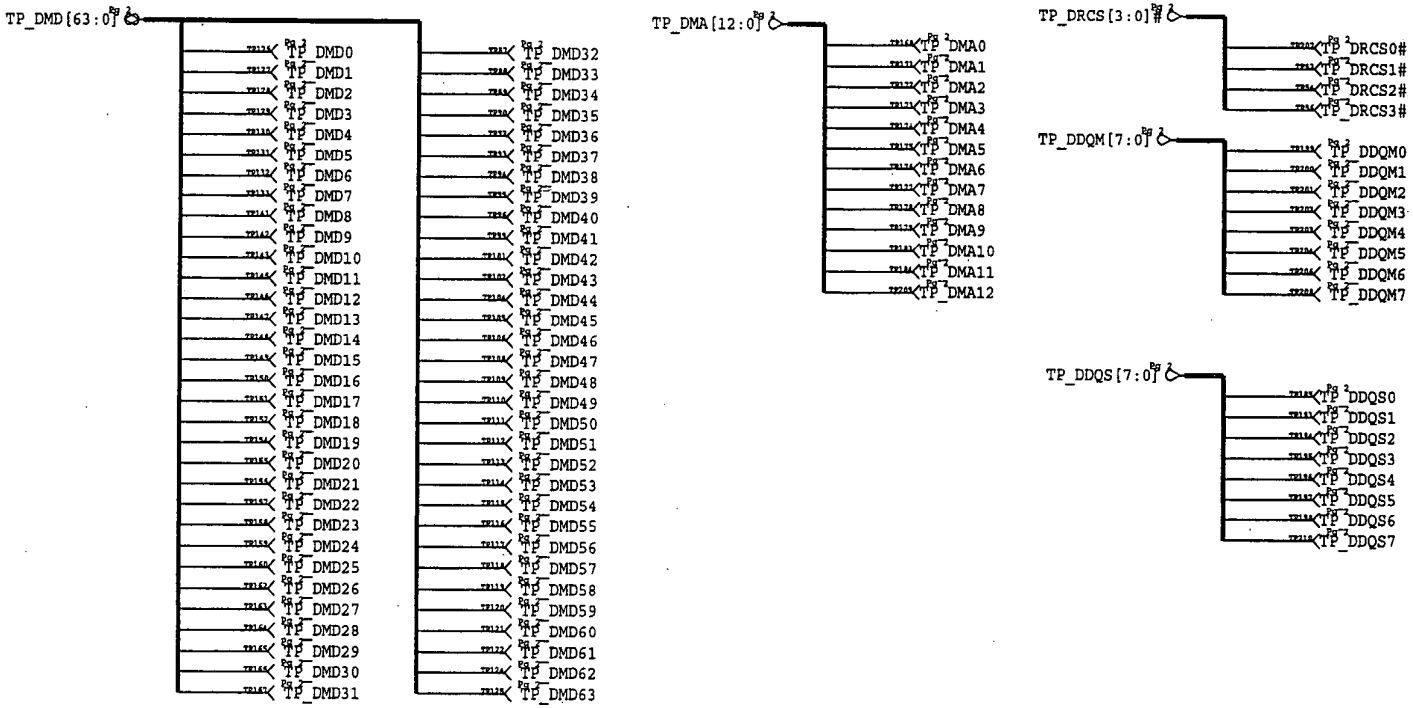

Page Title: Test points for unused DDR pins

Anigma Inc.

Title: RLXORB

Drawing Number: [redacted]

Release Date: [redacted]

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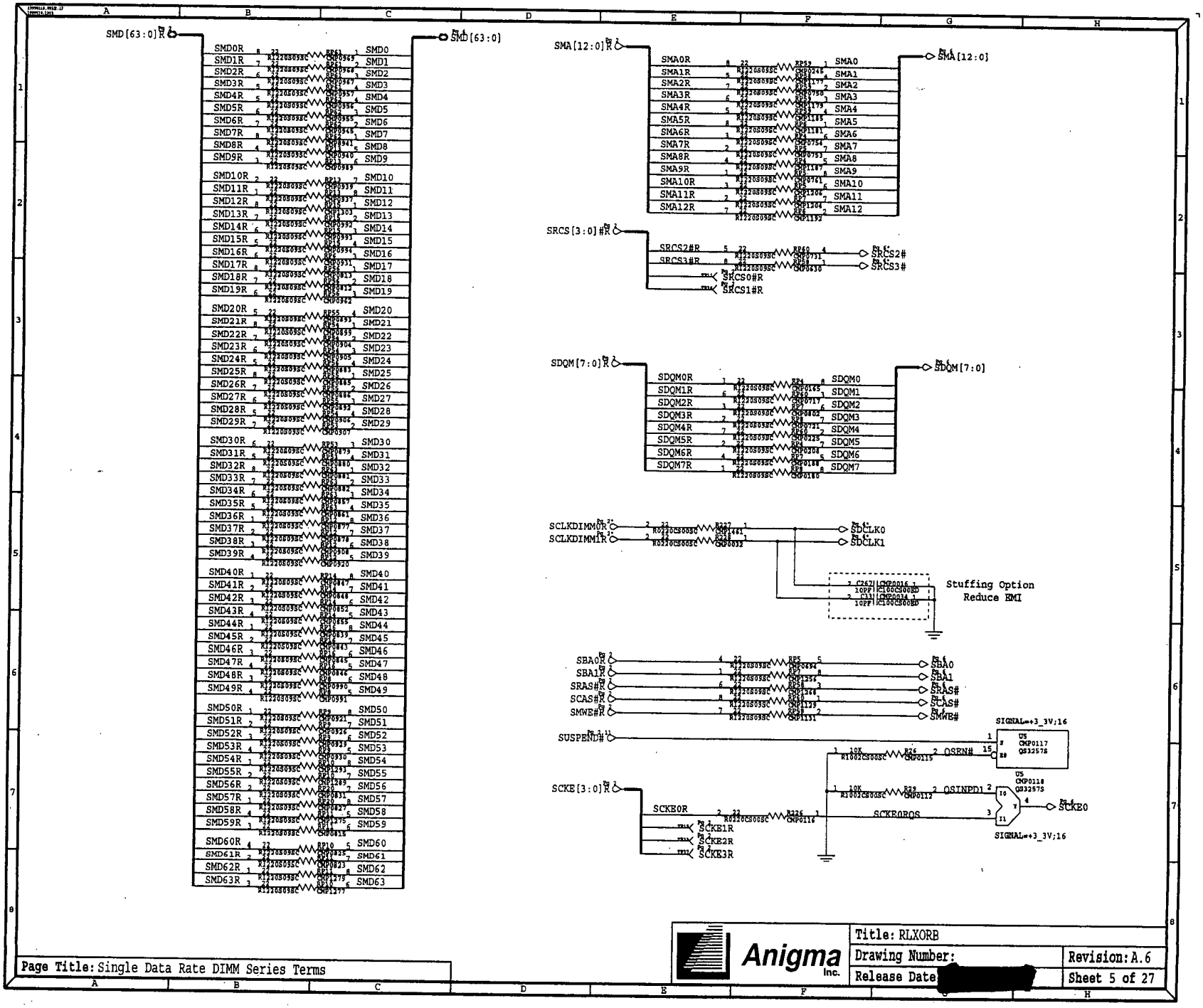

Page Title: Single Data Rate DIMM Series Terms

Anigma Inc.

Title: RLXORB

Drawing Number: [redacted]

Release Date: [redacted]

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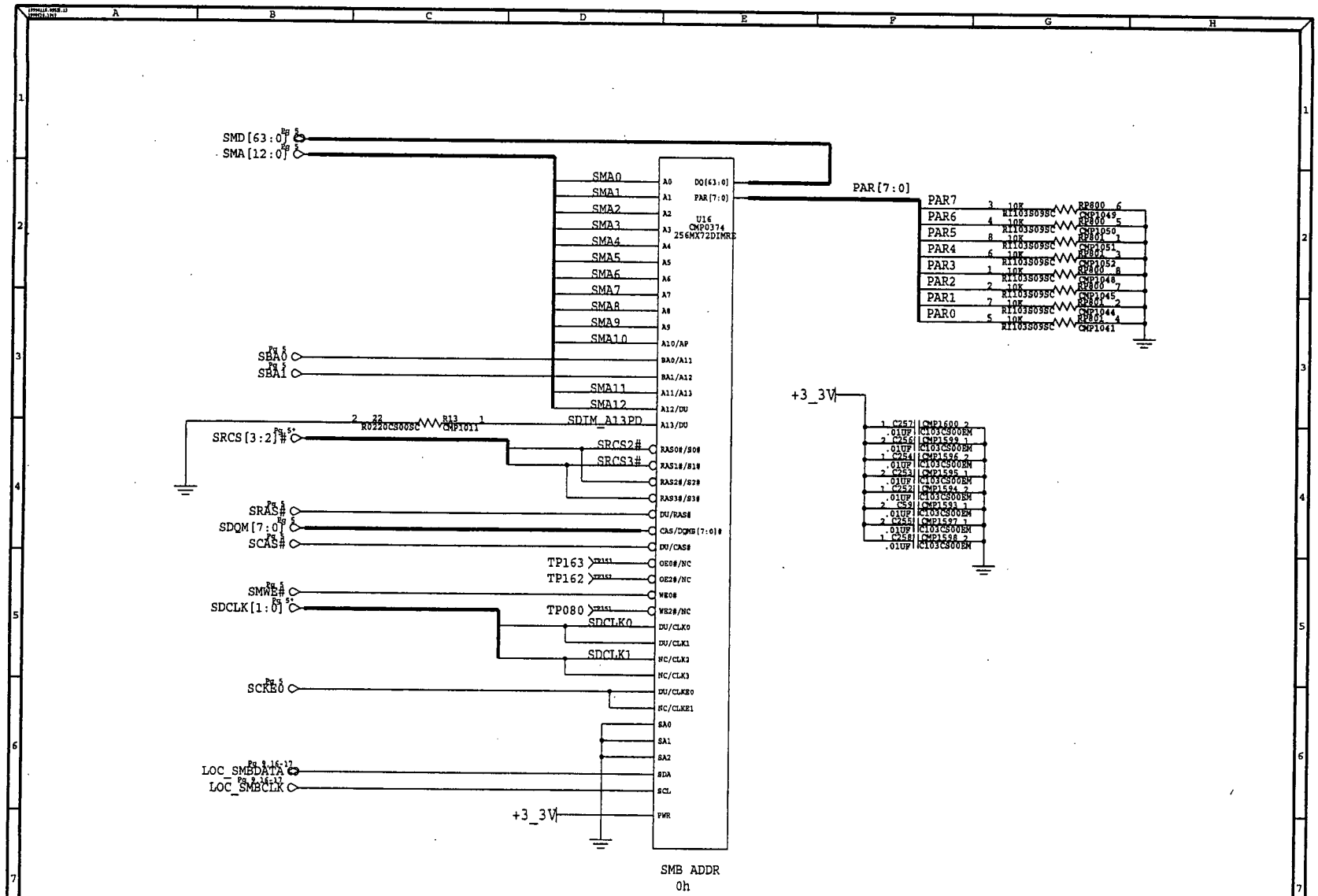

Page Title: DIMM Module

Anigma Inc.

Title: RLXORB	
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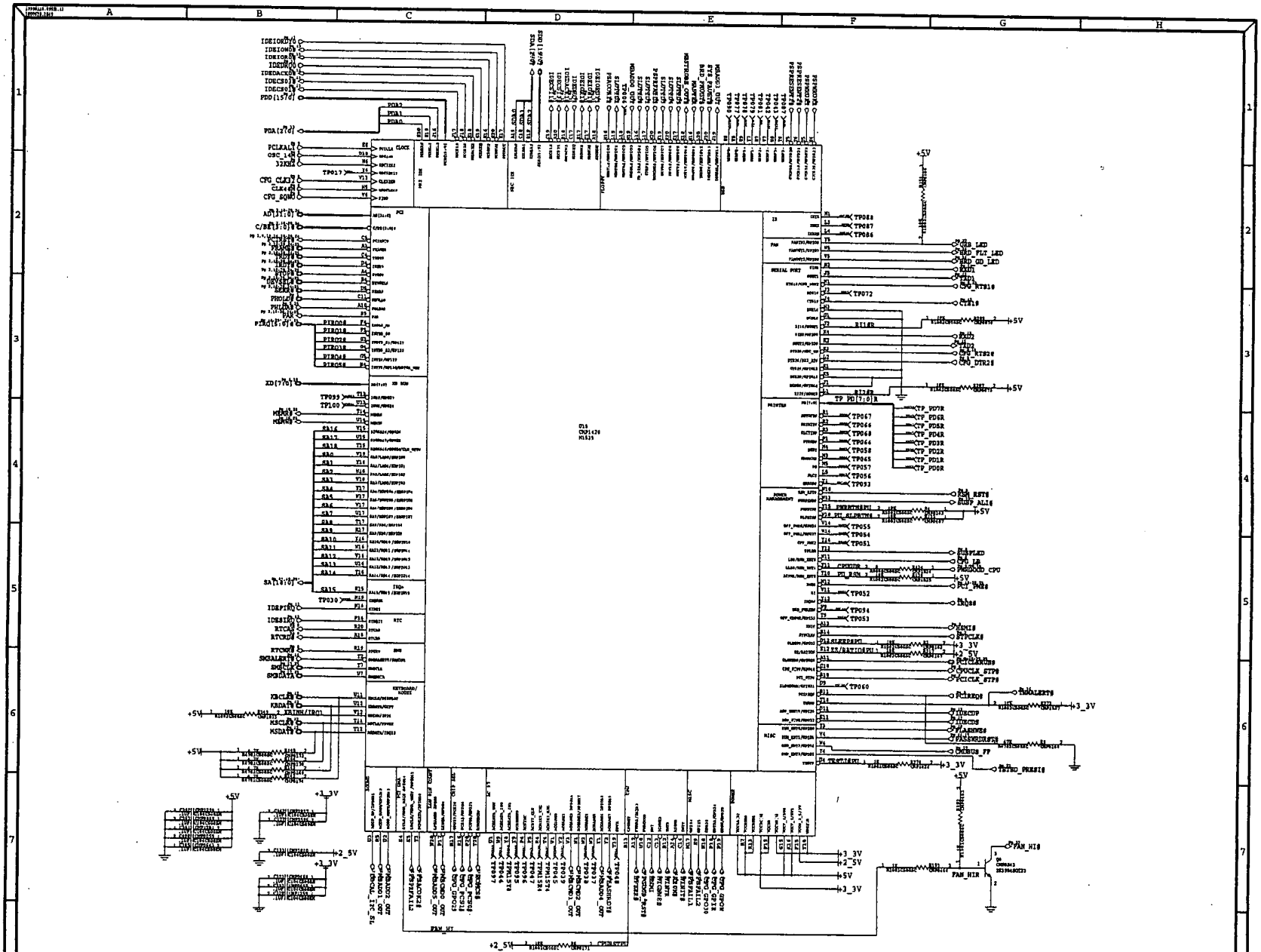

Page Title: M1535 South Bridge

Anigma Inc.

Title: RLXORB

Drawing Number:

Release Date: [redacted]

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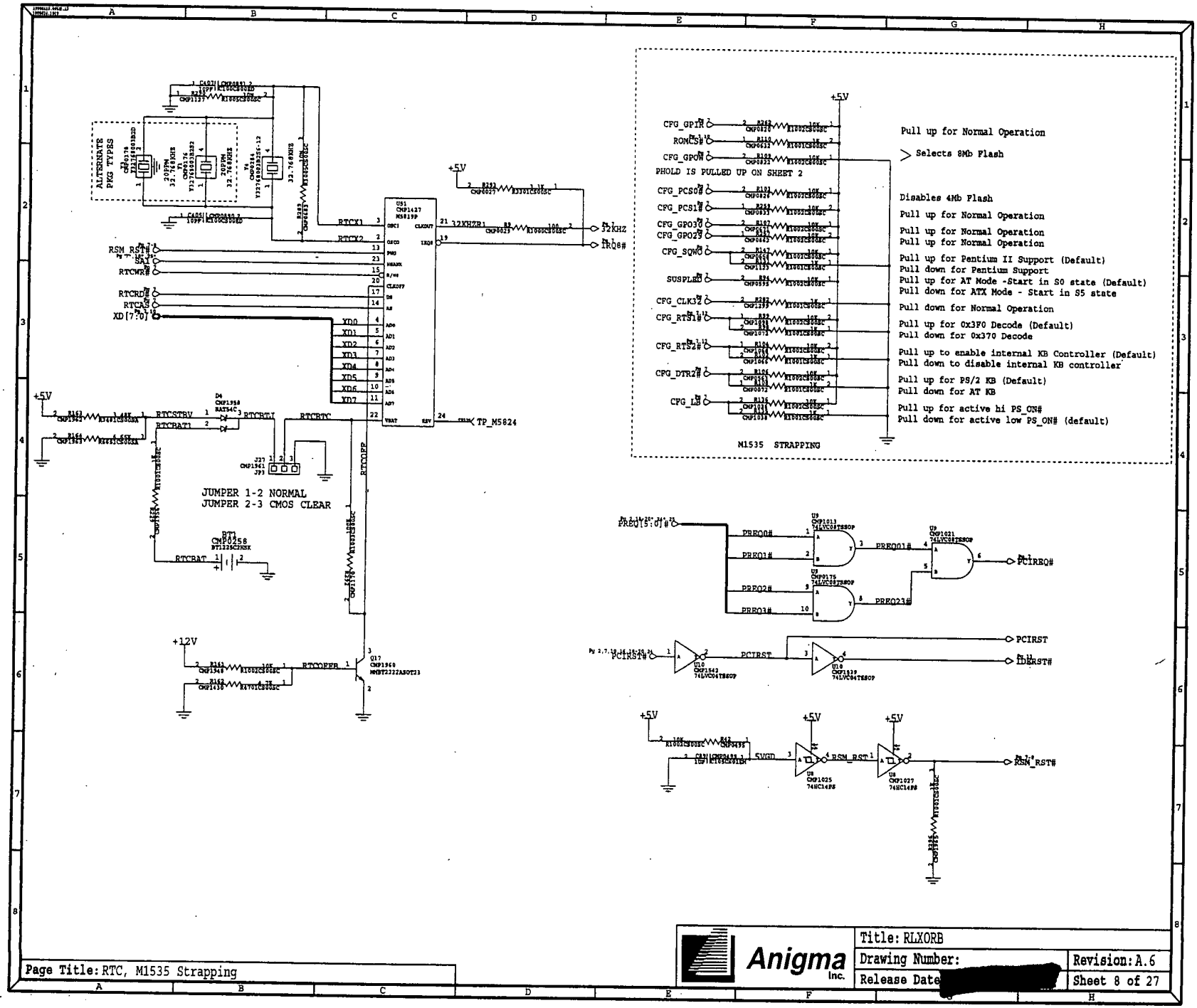

Page Title: RTC, M1535 Strapping

Anigma Inc.

Title: RLXORB

Drawing Number:

Release Date [redacted]

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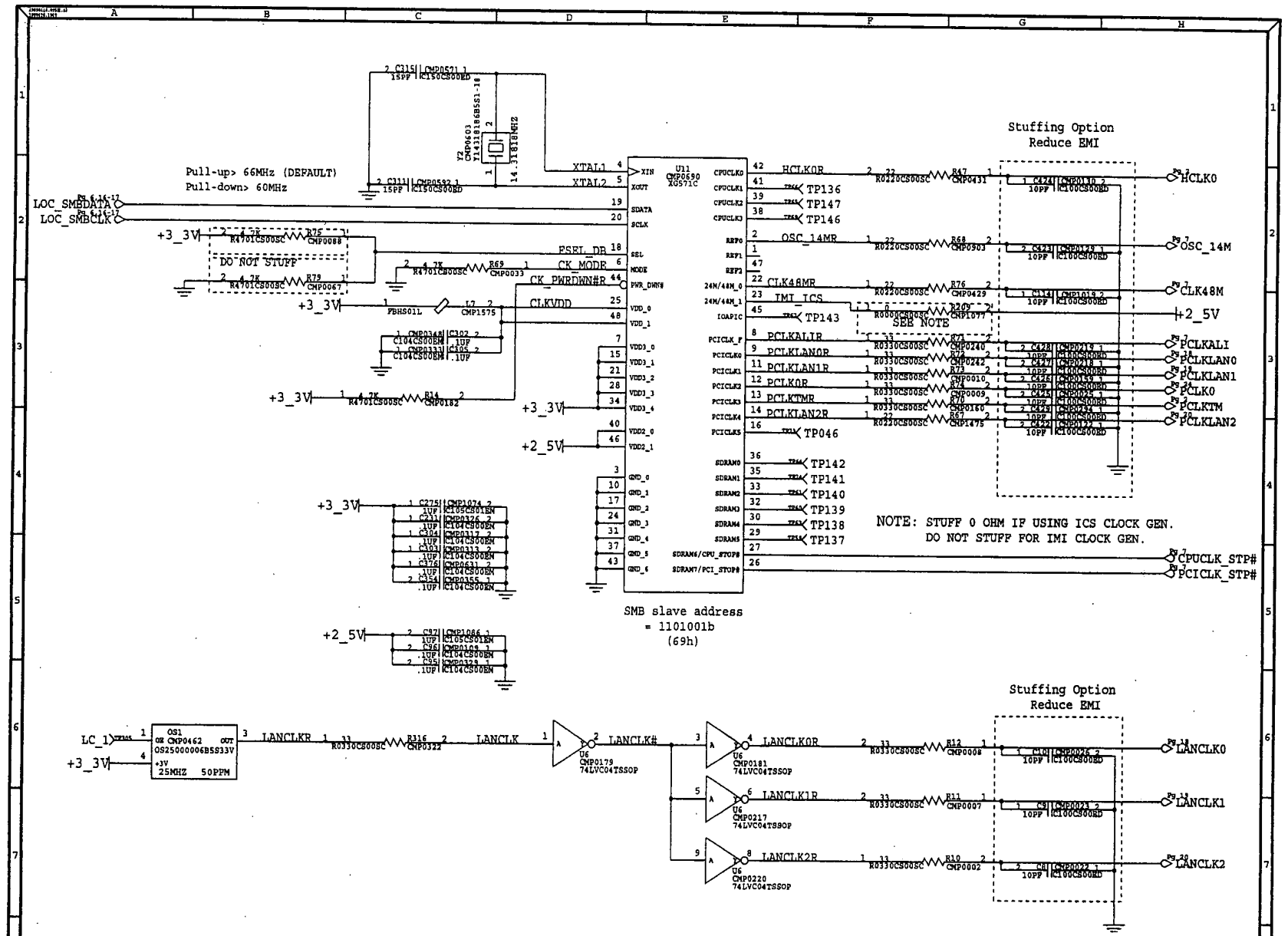

Page Title: Clock Generator

Anigma Inc.

Title: RLXORB

Drawing Number:

Revision: A.6

Release Date: [redacted]

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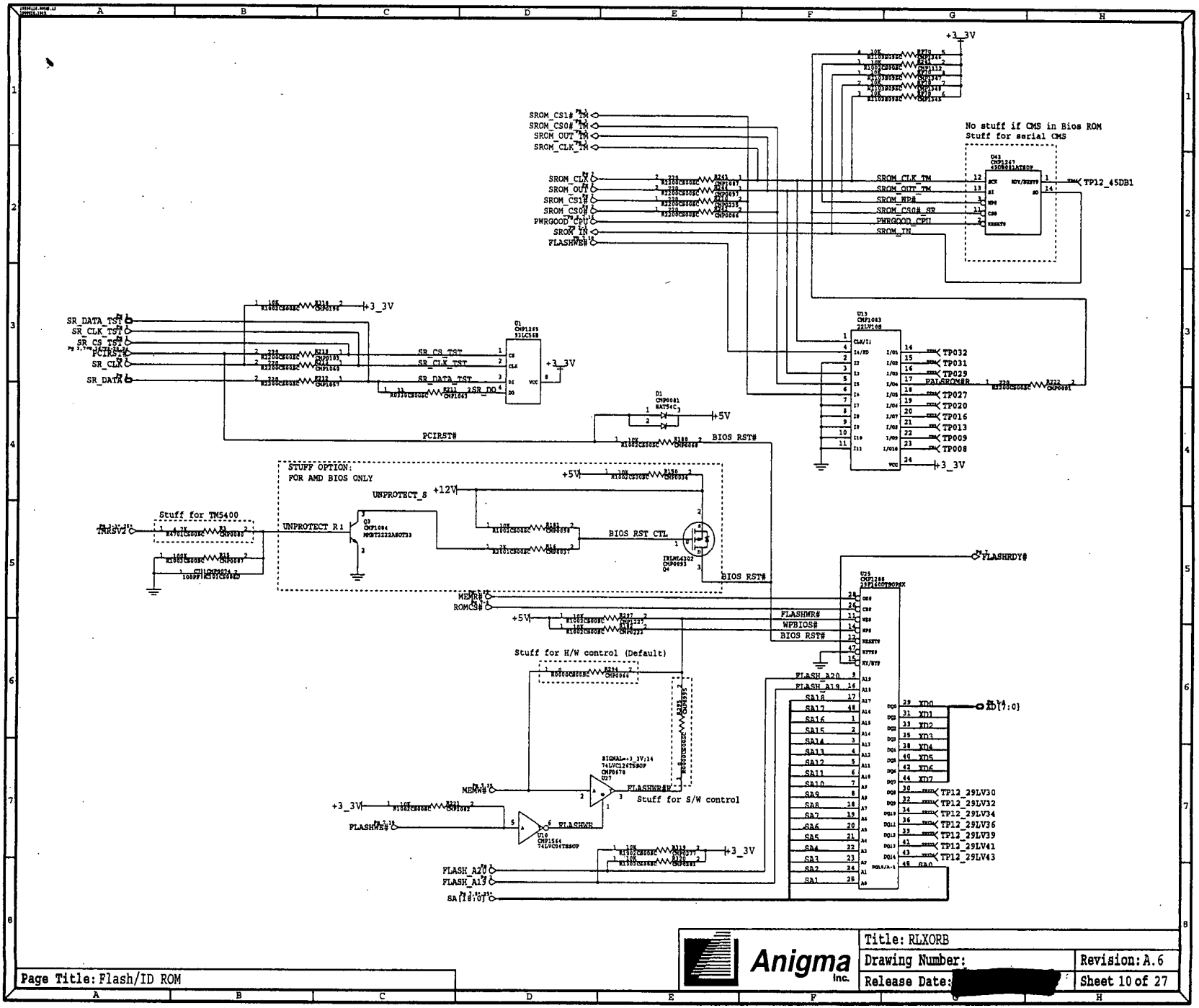

Anigma Inc.

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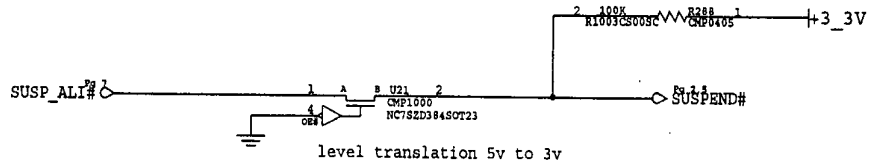
Page Title: Flash/ID ROM

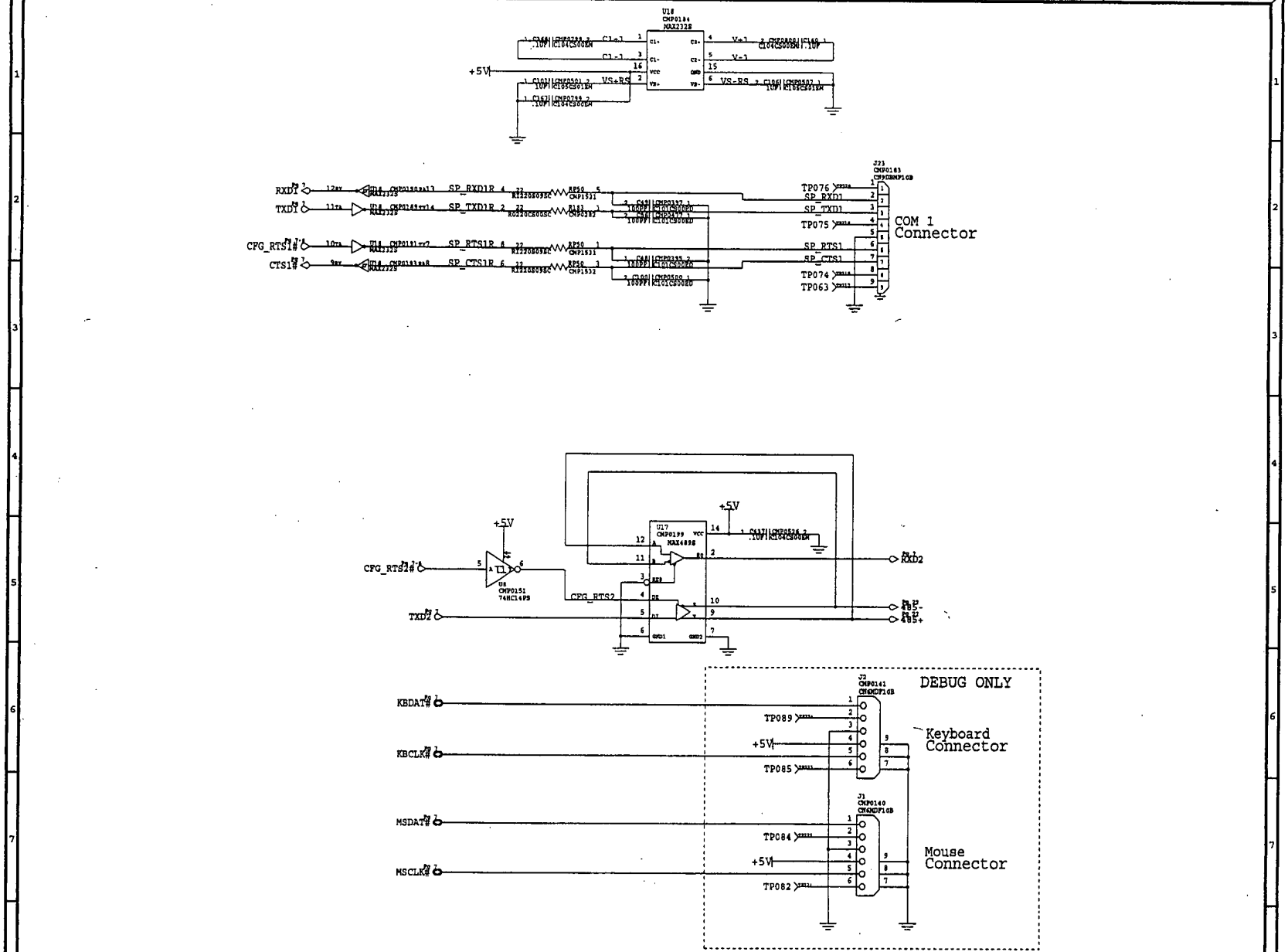


level translation 5v to 3v

Page Title: Suspend# Q-Switch

Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.6
Release Date: [redacted]	Sheet 11 of 27



Page Title: Serial Ports, RS-232, RS-485

Anigma Inc.

Title: RLXORB	
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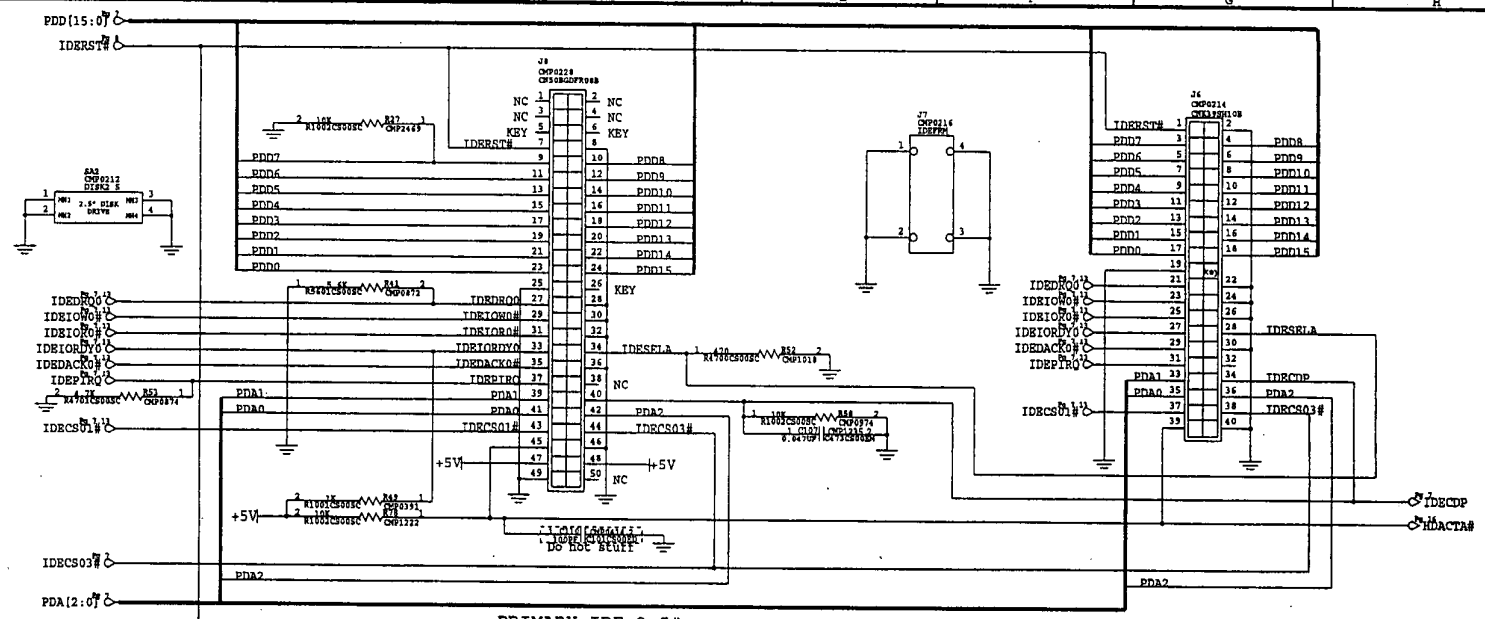

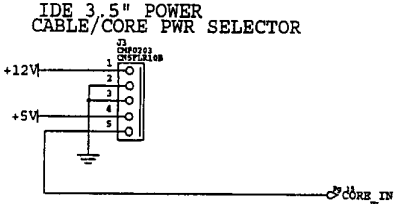

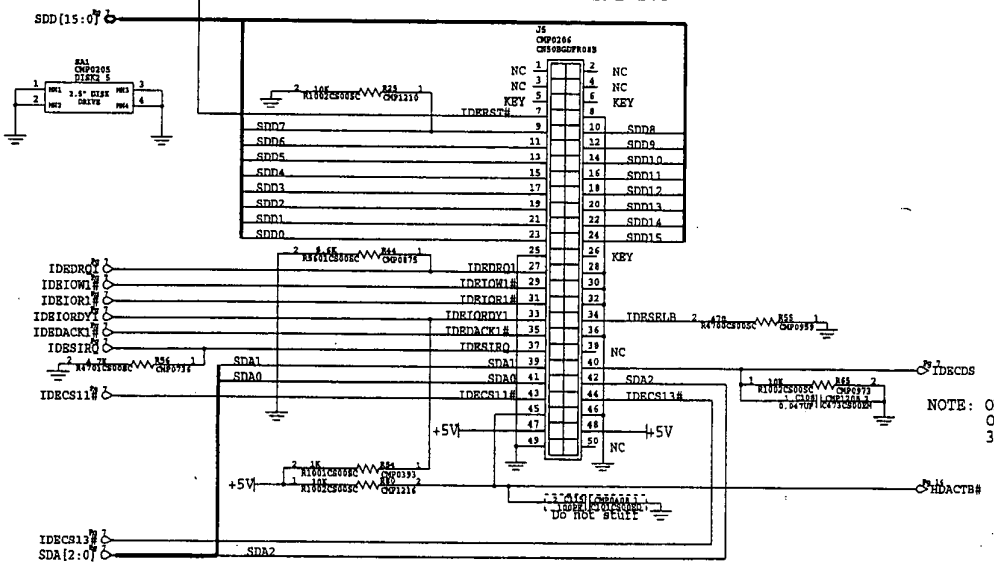

NOTE: ONLY 1-3.5" DRIVE WILL BE INSTALLED
OR 1 OR 2-2.5" DRIVES.
3.5" AND 2.5" AT THE SAME TIME IS NOT SUPPORTED.

Anigma Inc.	Title: RLXORB	
	Drawing Number:	Revision: A.6
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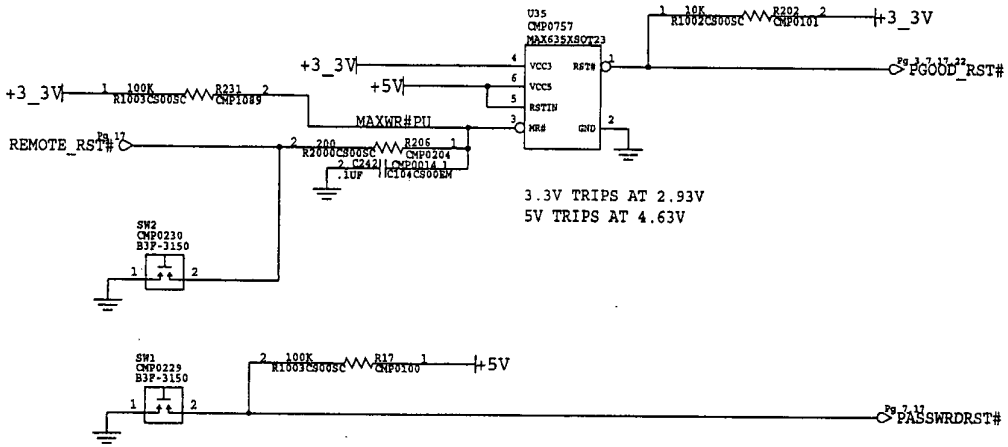
Page Title: IDE Interface



Page Title: Voltage Monitoring / Reset control

Anigma Inc.

Title: RLXORB

Drawing Number:

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Release Date [redacted]

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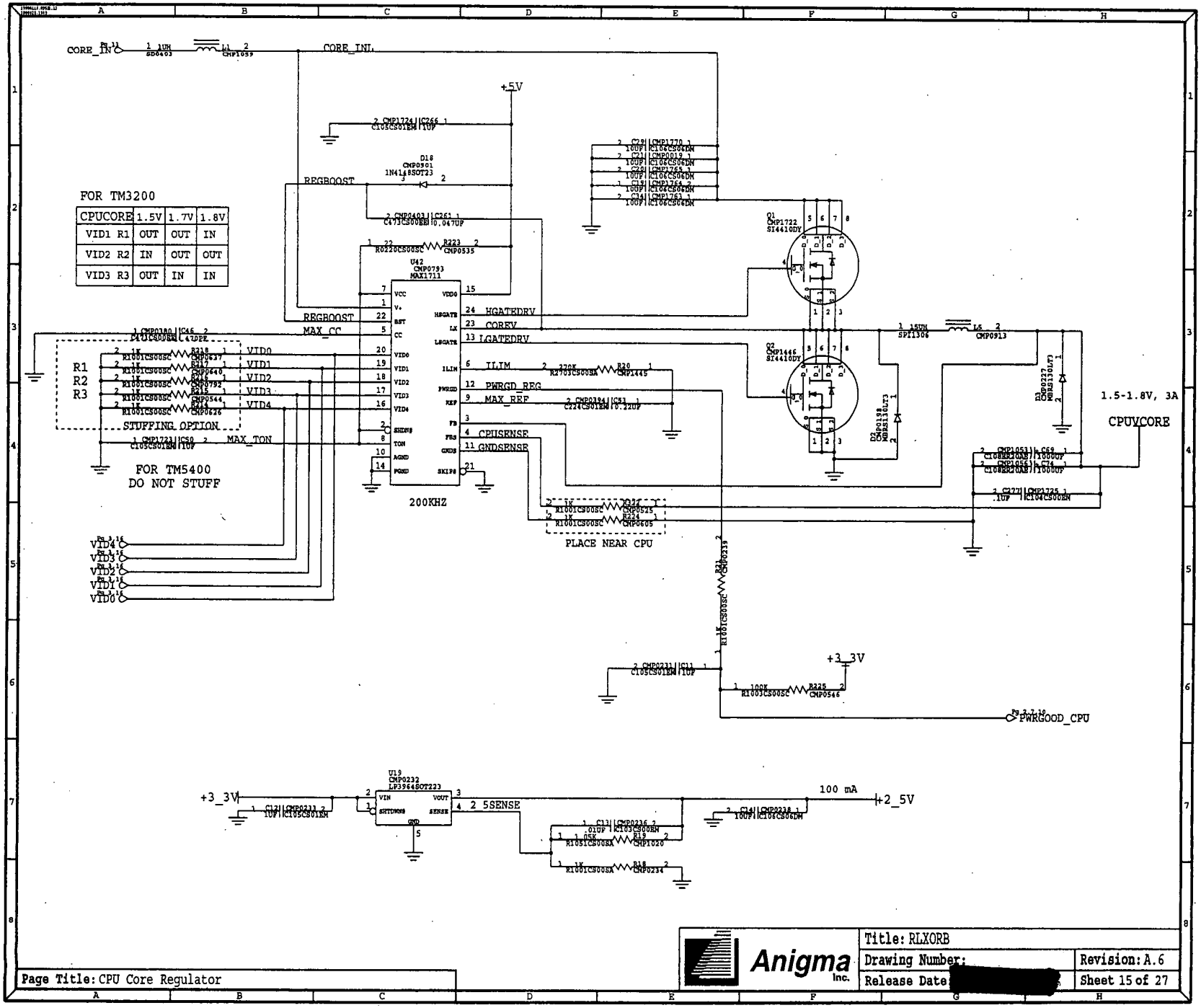

Page Title: CPU Core Regulator

Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.6
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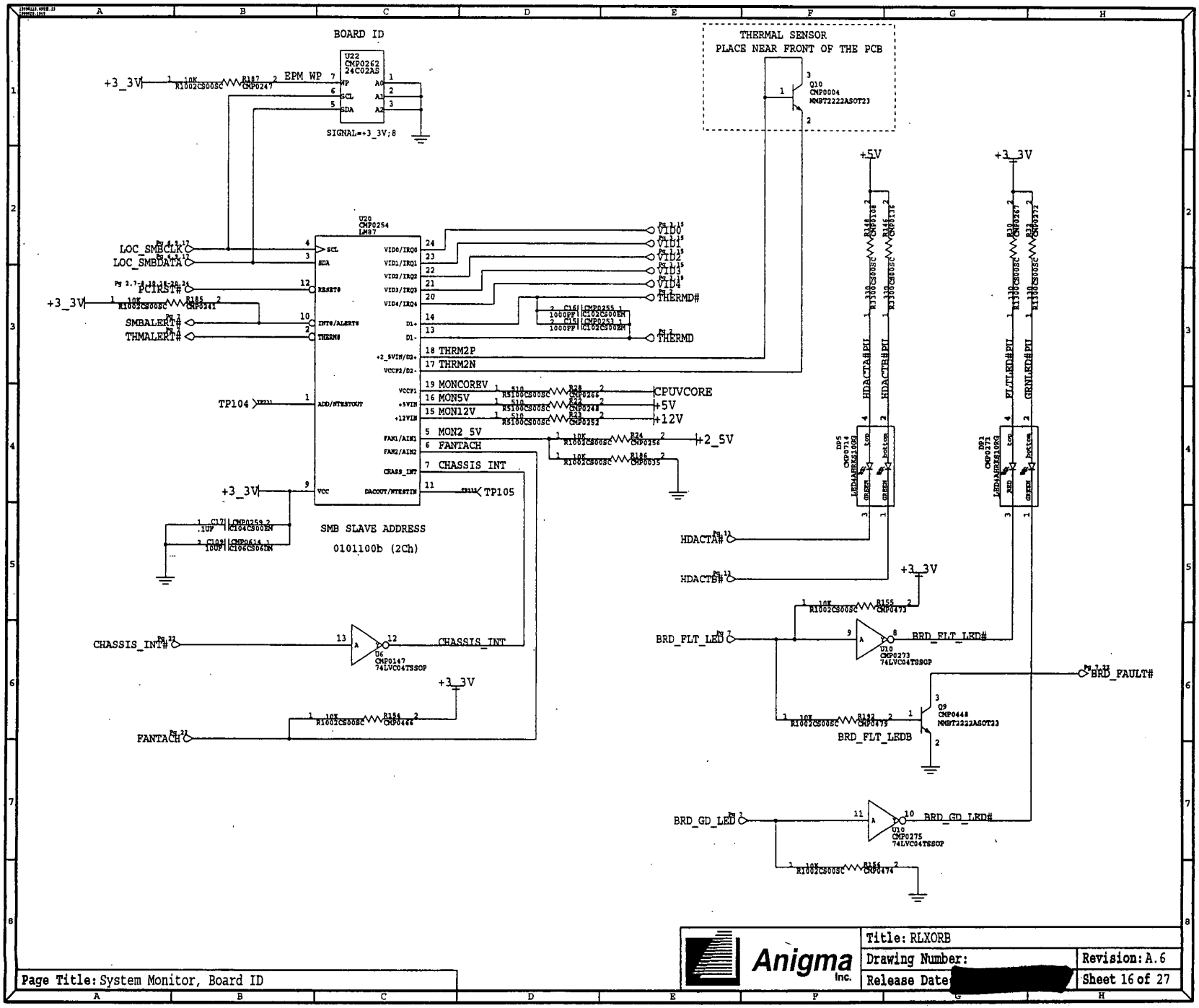

Anigma Inc.

Title: RLXORB

Drawing Number:

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Release Date: [redacted]

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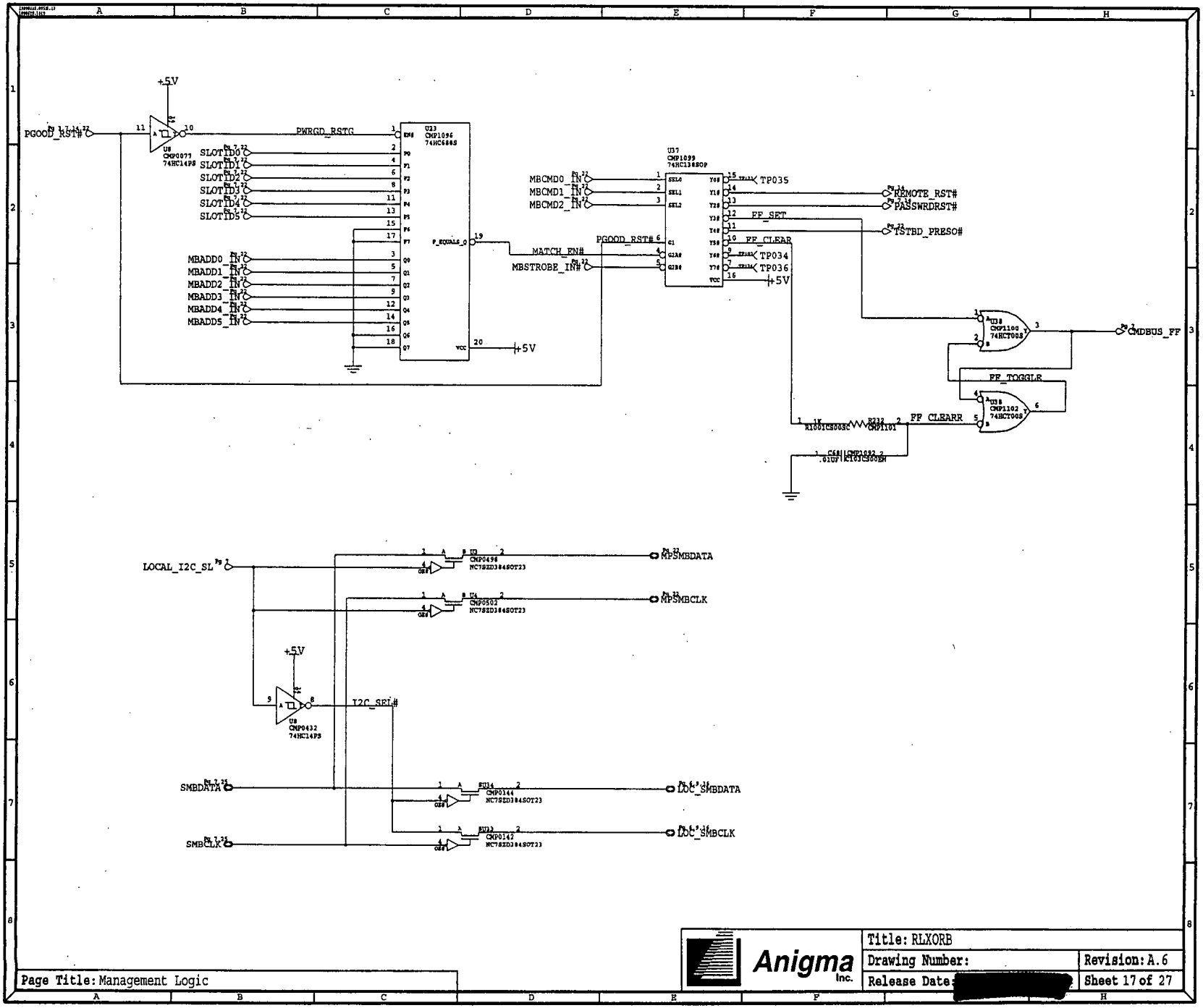
Page Title: System Monitor, Board ID



Page Title: Management Logic

Anigma Inc.

Title: RLXORB

Drawing Number:

Revision: A.6

Release Date: [redacted]

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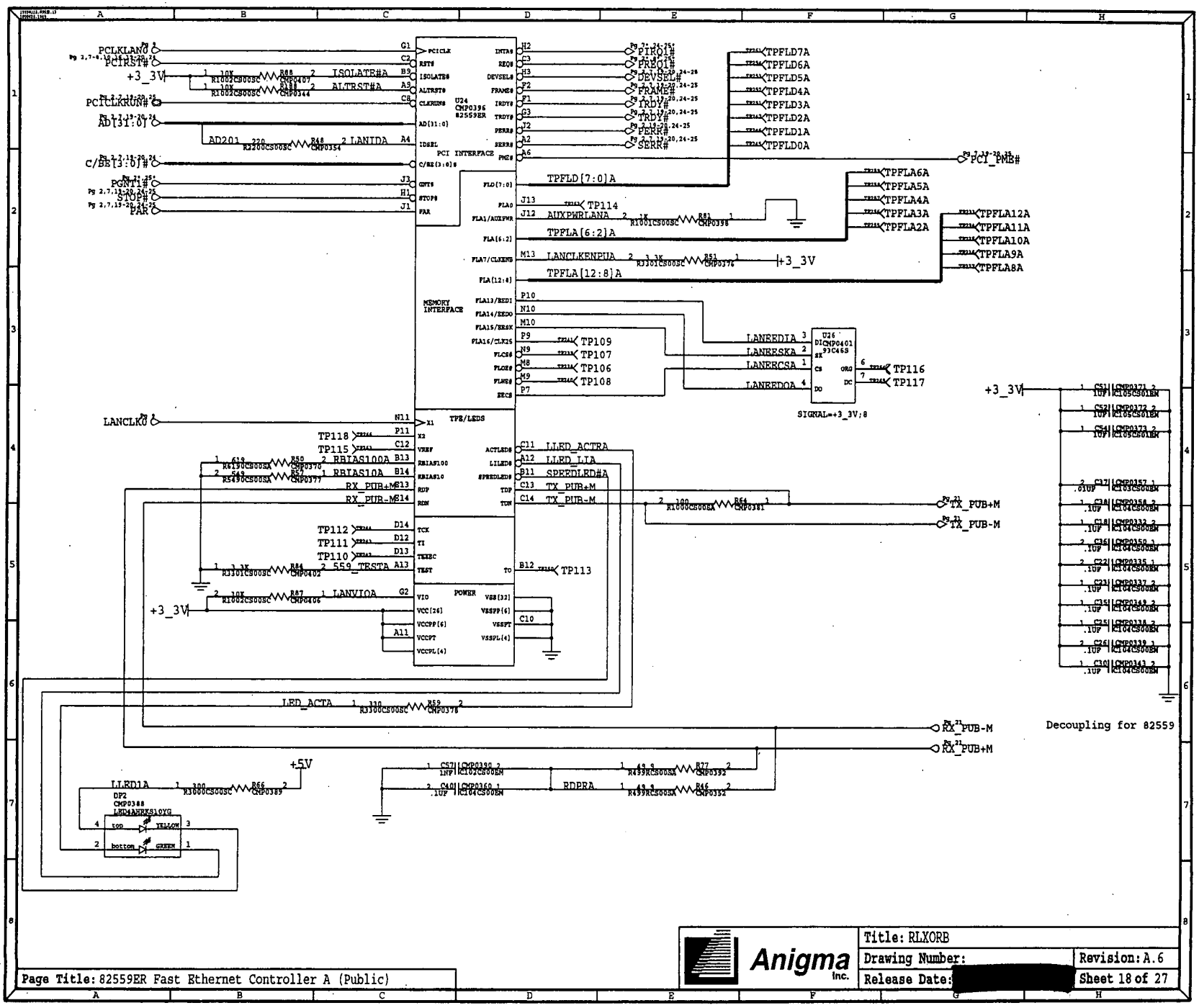

Anigma Inc.

Title: RLXORB

Drawing Number:

Revision: A.6

Release Date: [redacted]

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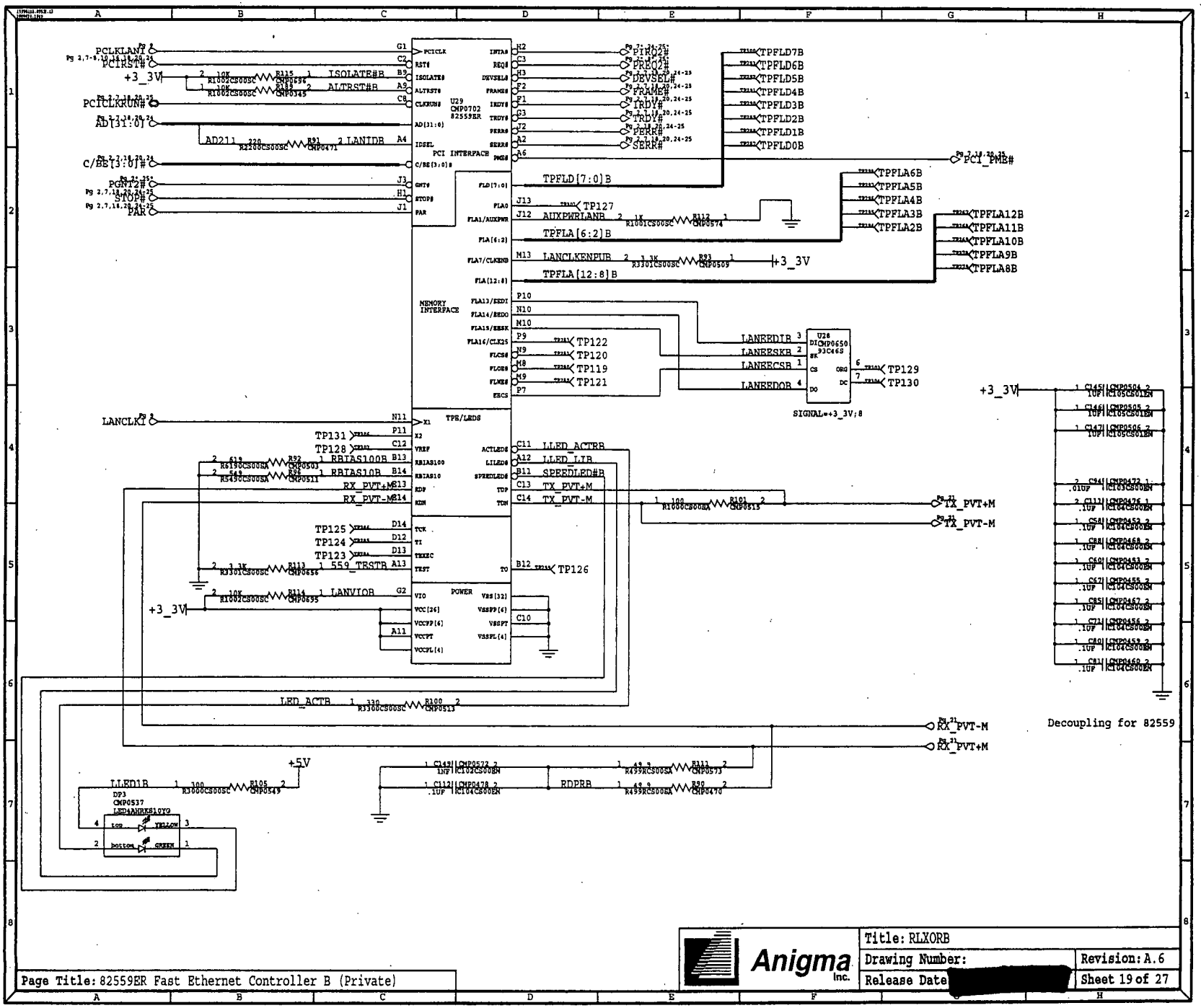
Page Title: 82559ER Fast Ethernet Controller A (Public)



Anigma Inc.

Title: RLXORB

Drawing Number:

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Release Date [redacted]

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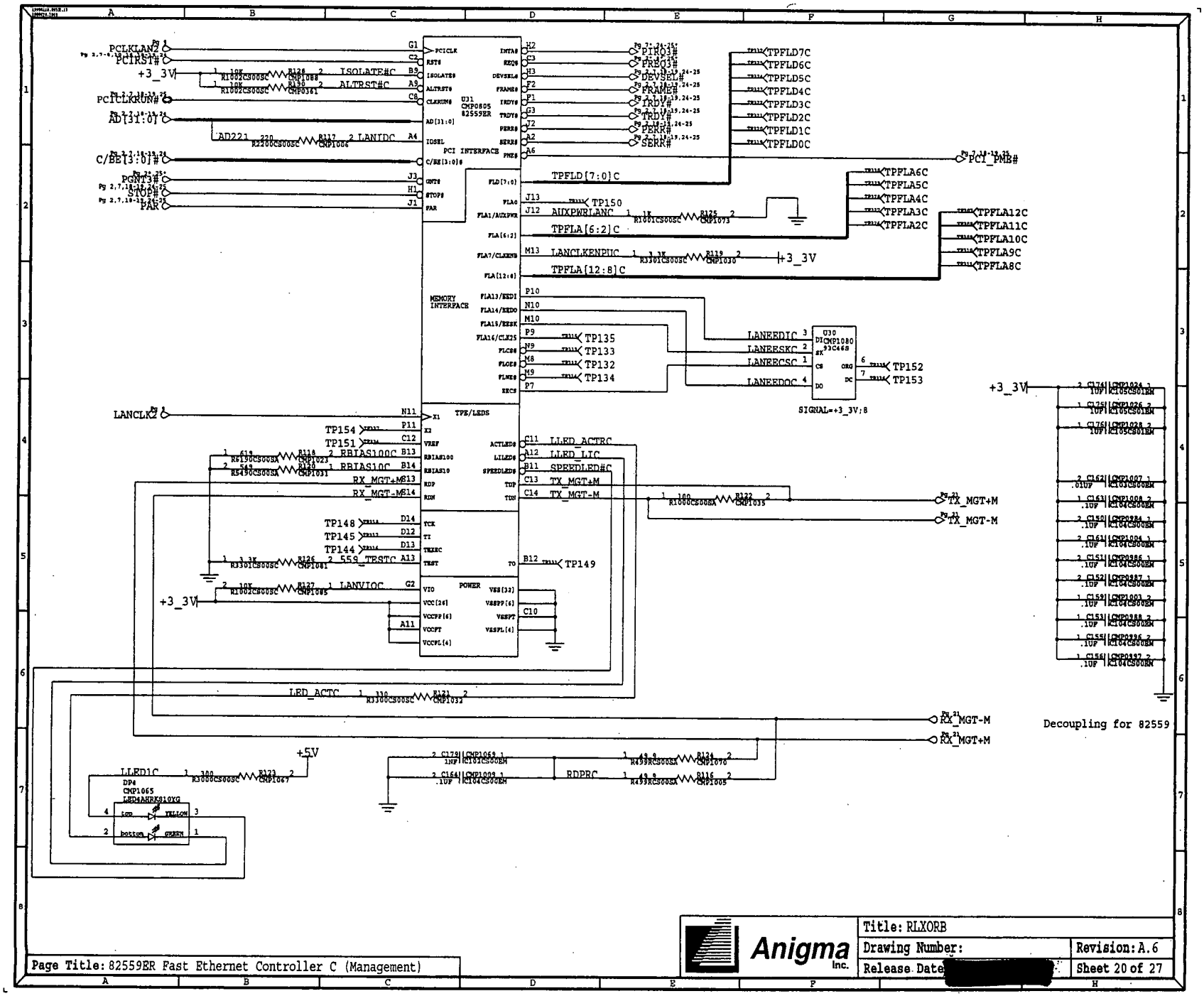
Page Title: 82559ER Fast Ethernet Controller B (Private)


PCLKLAN2
PCIRST#C
+3_3V
ISOLATE#C
ALTRST#C
PCICLKRUN#
AD[31:0]C
AD22
LANIDC
C/BE[3:0]#C
PGNT3#C
STOP#C
PAR
U31
CMP0805
82559ER
PCI INTERFACE
MEMORY INTERFACE
TPE/LEDS
POWER
PCICLK
RST#
ISOLATE#
ALTRST#
CLKRUN#
AD[31:0]
IDSEL
C/BE[3:0]#
GNT#
STOP#
PAR
INTA#
REQ#
DEVSEL#
FRAME#
IRDY#
TRDY#
PERR#
SERR#
PME#
FLD[7:0]
FLA0
FLA1/AUXPWR
FLA[6:2]
FLA7/CLKEN#
FLA[12:8]
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16/CLK25
FLCS#
FLOE#
FLWE#
EECS
X1
X2
VREF
RBIAS100
RBIAS10
RDP
RDN
TCK
TI
TMSRC
TEST
TO
ACTLED#
LILED#
SPEEDLED#
TDP
TDN
VIO
VCC[26]
VCCPP[6]
VCCPT
VCCPL[4]
VSS[32]
VSSPP[6]
VSSPT
VSSPL[4]
TPFLD[7:0]C
TPFLA[6:2]C
TPFLA[12:8]C
LANCLKENPUC
+3_3V
TP150
AUXPWRLANC
TP135
TP133
TP132
TP134
LANEEDIC
LANEESKC
LANEECSC
LANEEDOC
U30
DICMP1080
93C46B
TP152
TP153
SIGNAL=+3_3V;8
LANCLK2
TP154
TP151
RBIAS100C
RBIAS10C
RX_MGT+M
RX_MGT-M
TP148
TP145
TP144
TESTC
TP149
LANVIOC
LED_ACTC
LLED_ACTRC
LLED_LIC
SPEEDLED#C
TX_MGT+M
TX_MGT-M
RX_MGT-M
RX_MGT+M
RDPRC
+5V
LLED1C
DP4
CMP1065
LED4AHRK810YG
top
botton
YELLOW
GREEN
Decoupling for 82559
Anigma Inc.
Title: RLXORB
Drawing Number:
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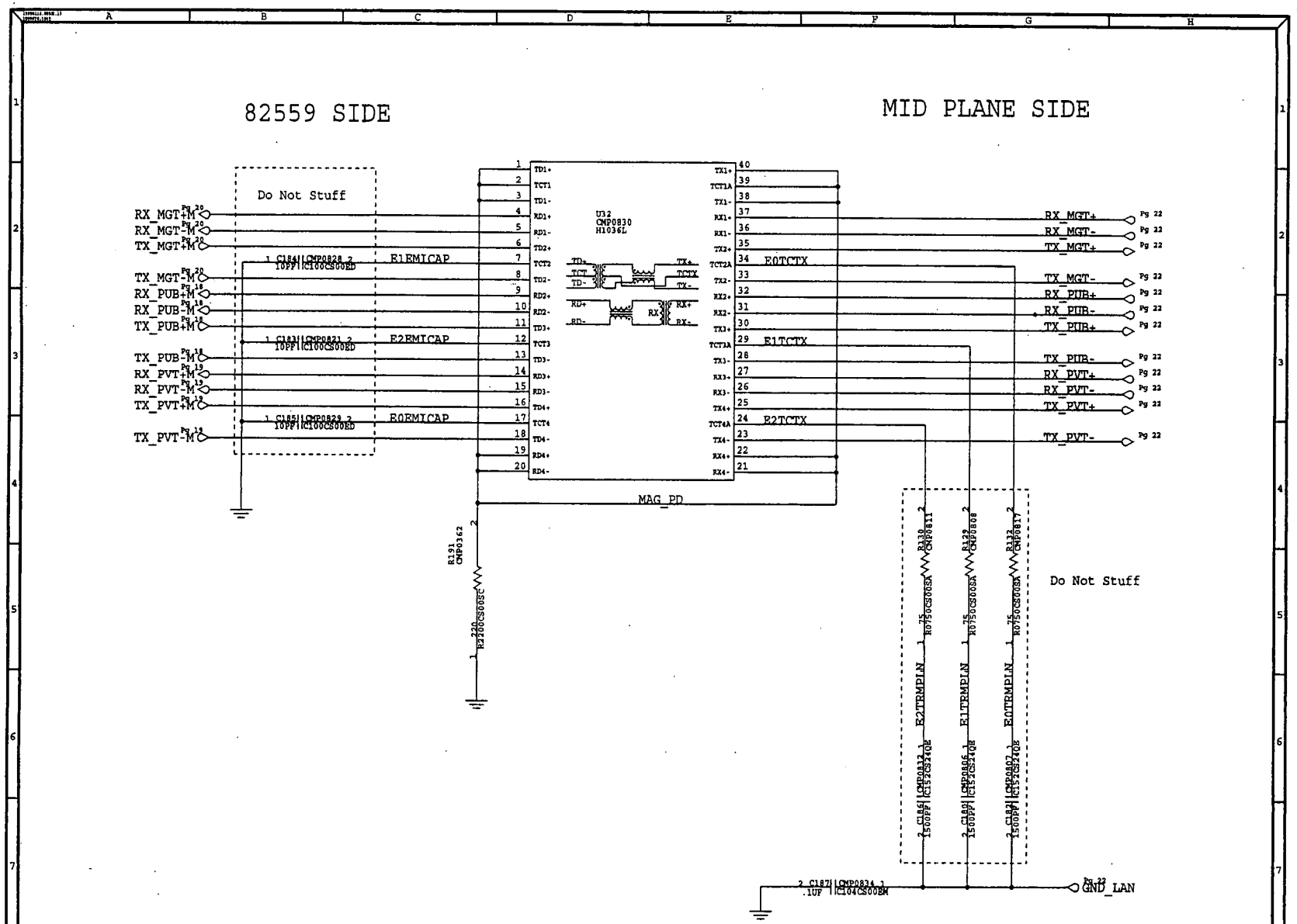
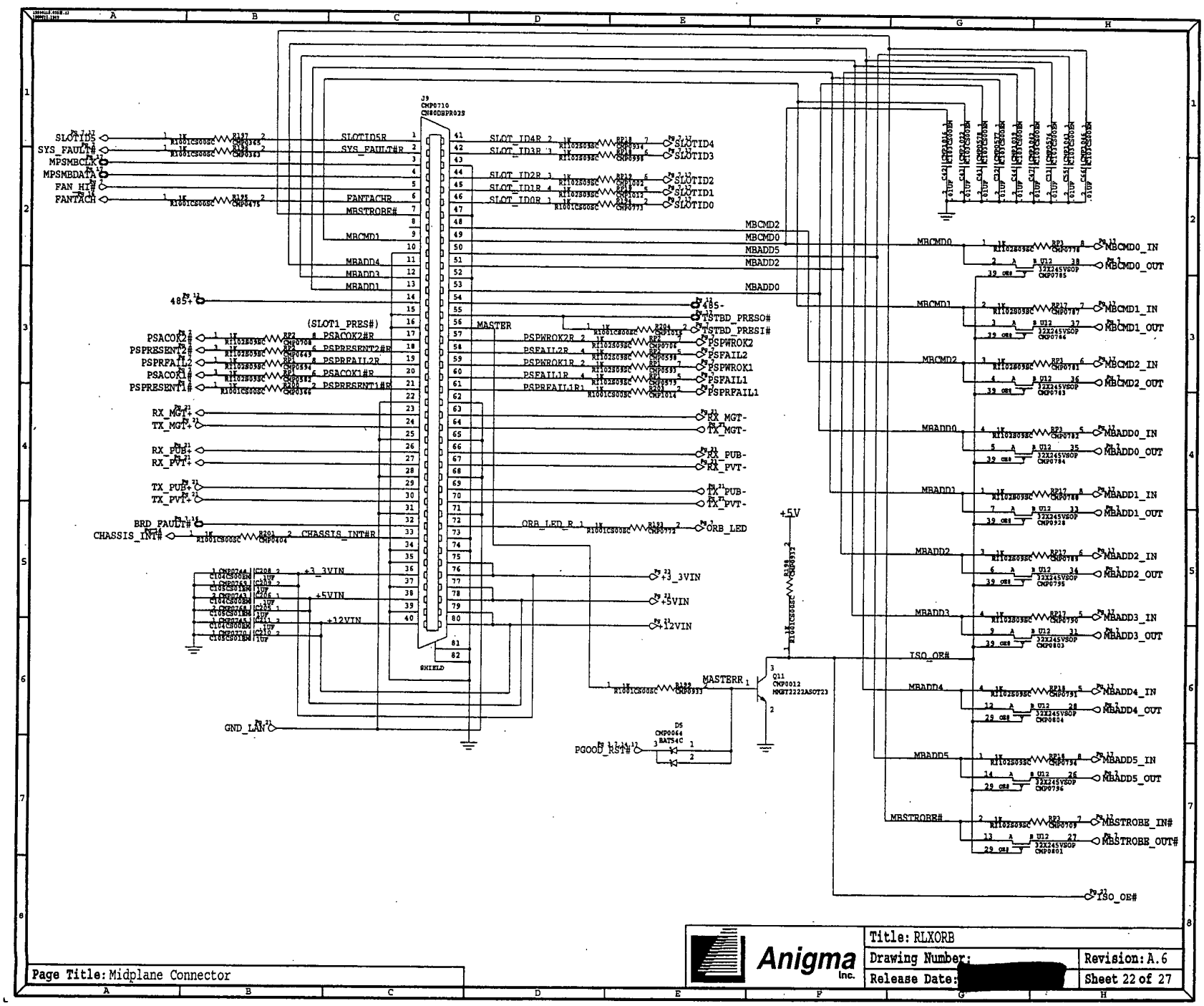
Release Date
Sheet 20 of 27
Page Title: 82559ER Fast Ethernet Controller C (Management)



Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.6
Release Date: [redacted]	Sheet 21 of 27

Page Title: Lan Magnetics



Anigma Inc.

Title: RLXORB

Drawing Number: [redacted]

Revision: A.6

Release Date: [redacted]

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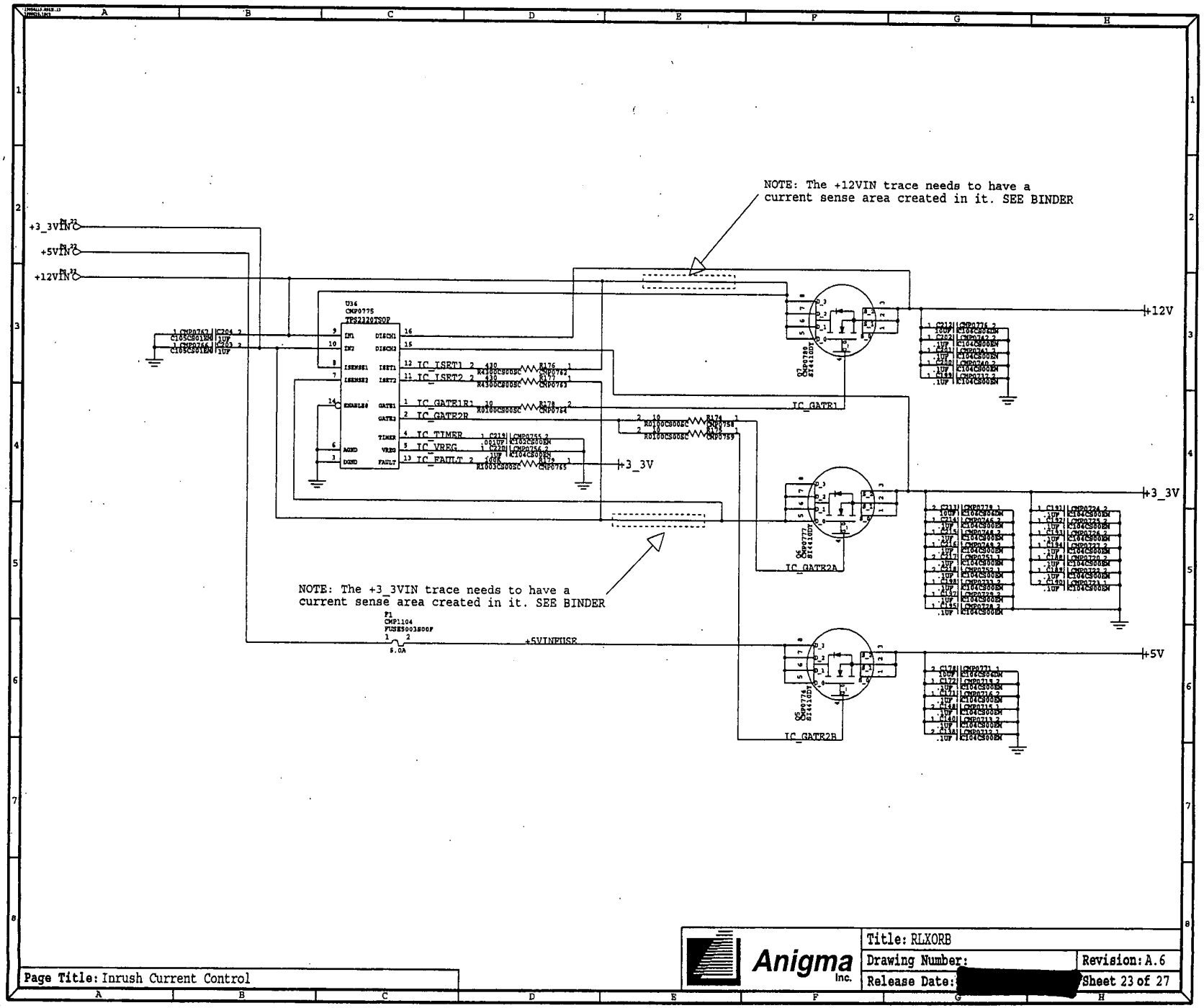
Page Title: Midplane Connector


NOTE: The +12VIN trace needs to have a current sense area created in it. SEE BINDER
+3_3VIN
+5VIN
+12VIN
U36
CMP0775
TPS2120TSOP
IC_ISET1
IC_ISET2
IC_GATE1R1
IC_GATE2R
IC_TIMER
IC_VREG
IC_FAULT
IC_GATE1
IC_GATR2A
IC_GATR2B
+12V
+3_3V
+5V
NOTE: The +3_3VIN trace needs to have a current sense area created in it. SEE BINDER
F1
CMP1104
FUSE5003800F
5.0A
+5VINFUSE
Anigma Inc.
Title: RLXORB
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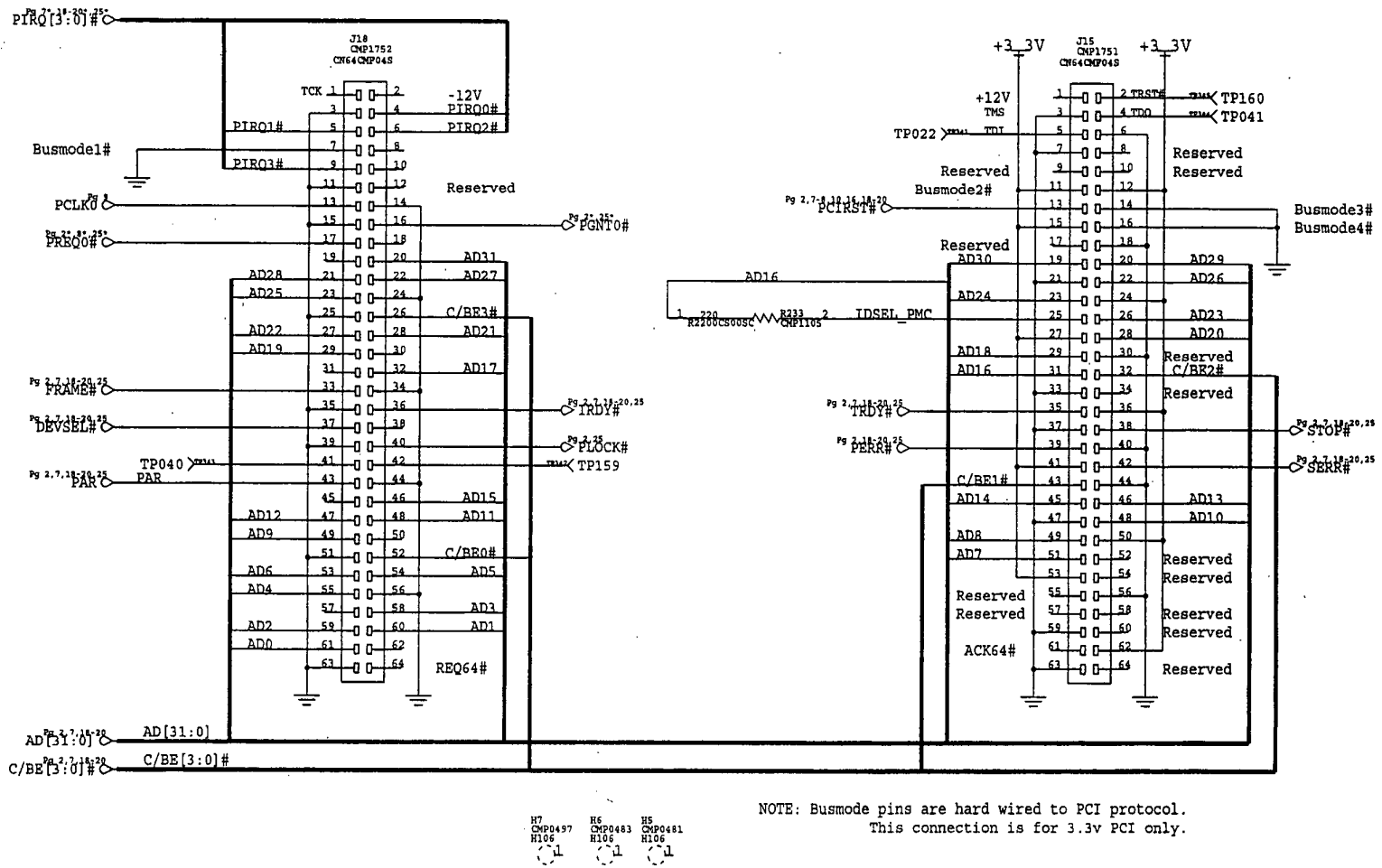
Release Date:
Sheet 23 of 27
Page Title: Inrush Current Control



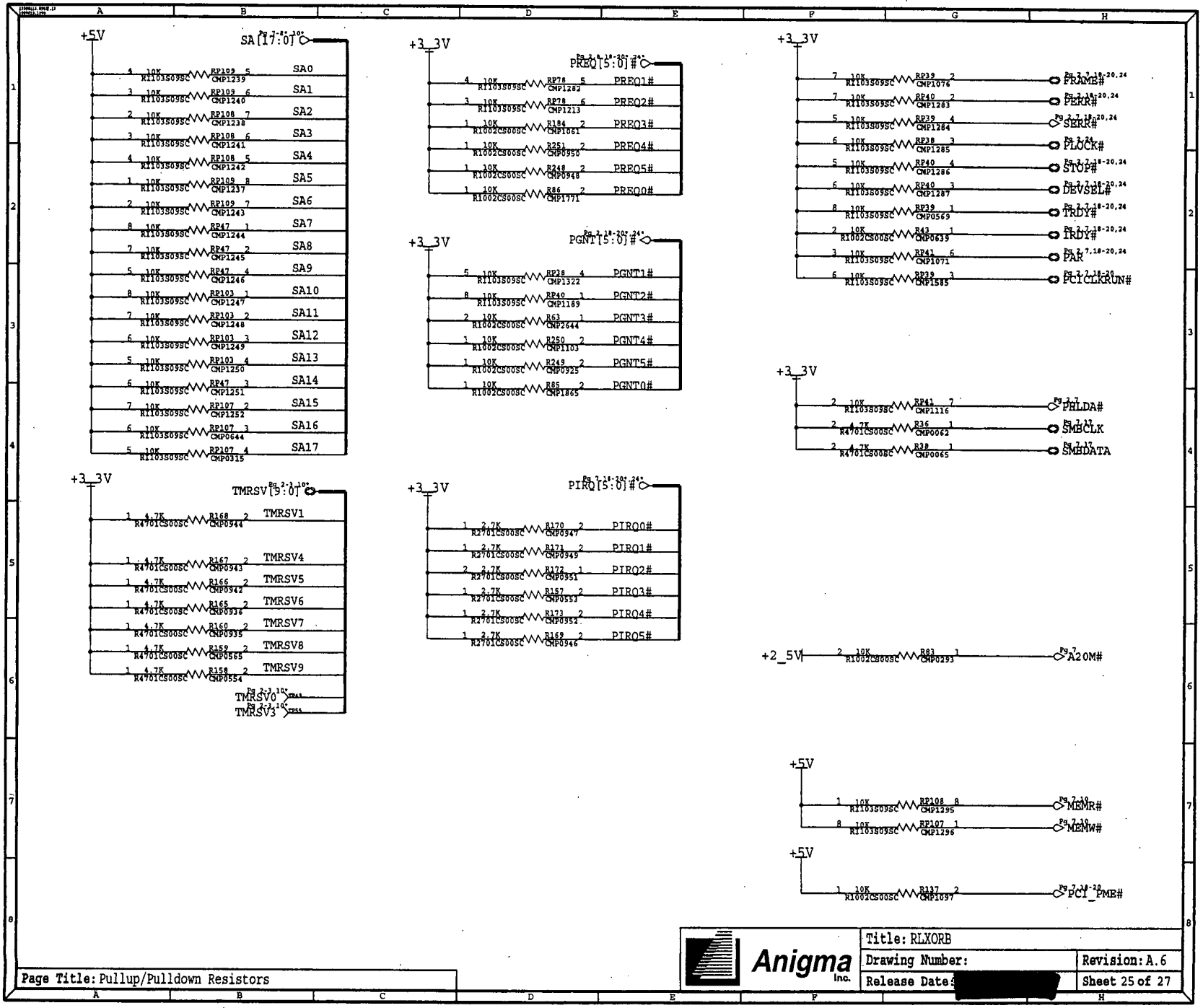
NOTE: Busmode pins are hard wired to PCI protocol.
This connection is for 3.3v PCI only.

PMC CONNECTORS

Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.6
Release Date: [redacted]	Sheet 24 of 27

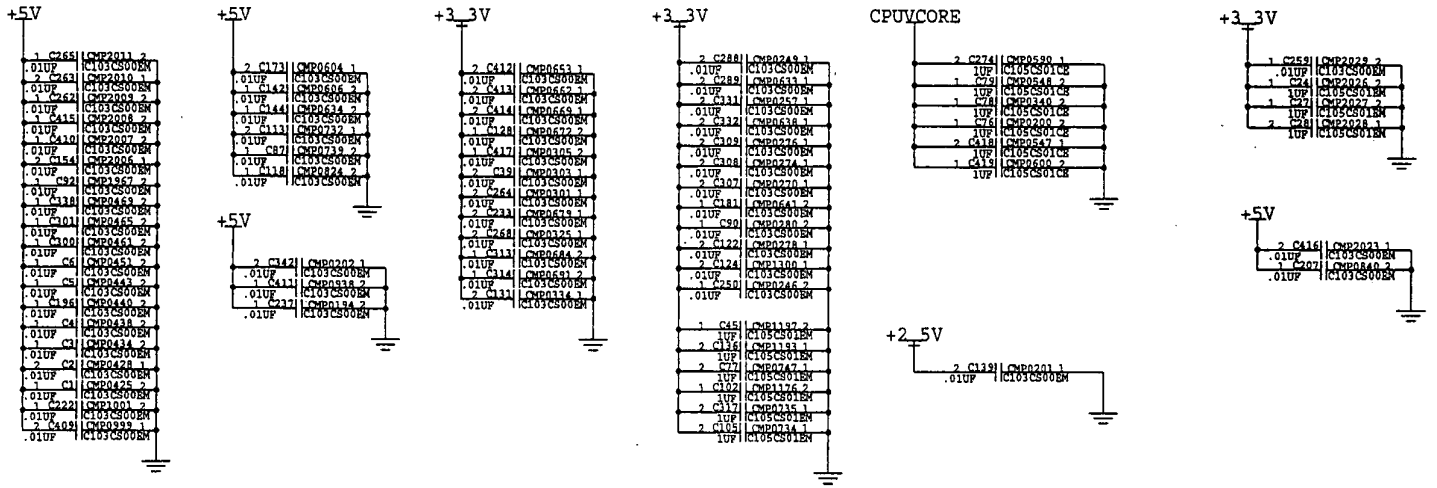
Page Title: PMC Debug Connectors



Page Title: Pullup/Pulldown Resistors

Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.6
Release Date: [redacted]	Sheet 25 of 27



Page Title: Decoupling Capacitors

Anigma Inc.

Title: RLXORB	
Drawing Number:	Revision: A.6
Release Date: [redacted]	Sheet 26 of 27

Ejector Hole

H1
CMP0382
H53

Fiducial Marks

FM1
CMP1489
FM200B

GF1
CMP1491
FM200B

GF2
CMP1490
FM200B

GF3
CMP1496
FM200B

GP4
CMP8000
FM200B

GP5
CMP8001
FM200B

GP6
CMP8002
FM200B

Tooling Holes

H3
CMP0954
H125

H4
CMP0956
H125

H2
CMP0953
H125

1K RT102S09SC RP19 CMP1133
1K RT102S09SC RP18 CMP1146
10K RT103S09SC RP41 CMP1147
10K RT103S09SC RP41 CMP1148
10K RT103S09SC RP28 CMP1149
10K RT103S09SC RP28 CMP1150
220 RT221S09SC RP21 CMP1157

+5V

U38
CMP1135
74HCT00S

U38
CMP1136
74HCT00S

TP071
TP070

U5
CMP1153
QS3257S
SIGNAL=+3_3V;16
TP161

U5
CMP1152
QS3257S
SIGNAL=+3_3V;16
TP083

U5
CMP1151
QS3257S
SIGNAL=+3_3V;16
TP091

TP158
TP156
SIGNAL=+3_3V;14
74LVC126TSSOP
CMP1143
U27

TP157
TP155
SIGNAL=+3_3V;14
74LVC126TSSOP
CMP1144
U27

TP102
TP103
SIGNAL=+3_3V;14
74LVC126TSSOP
CMP1145
U27

U6
CMP1154
74LVC04TSSOP
TP101

U10
CMP1155
74LVC04TSSOP
TP098

ISO_OE#

U12
32X245VSOP
CMP1138
TP069

U12
32X245VSOP
CMP1139
TP062

U12
32X245VSOP
CMP1140
TP061

U12
32X245VSOP
CMP1141
TP059

U12
32X245VSOP
CMP1134
TP050

U12
32X245VSOP
CMP1142
TP049

U9
CMP1156
74LVC08TSSOP
TP092

+5V

U8
CMP1137
74HC14PS
TP073

Anigma Inc.

Title: RLXORB
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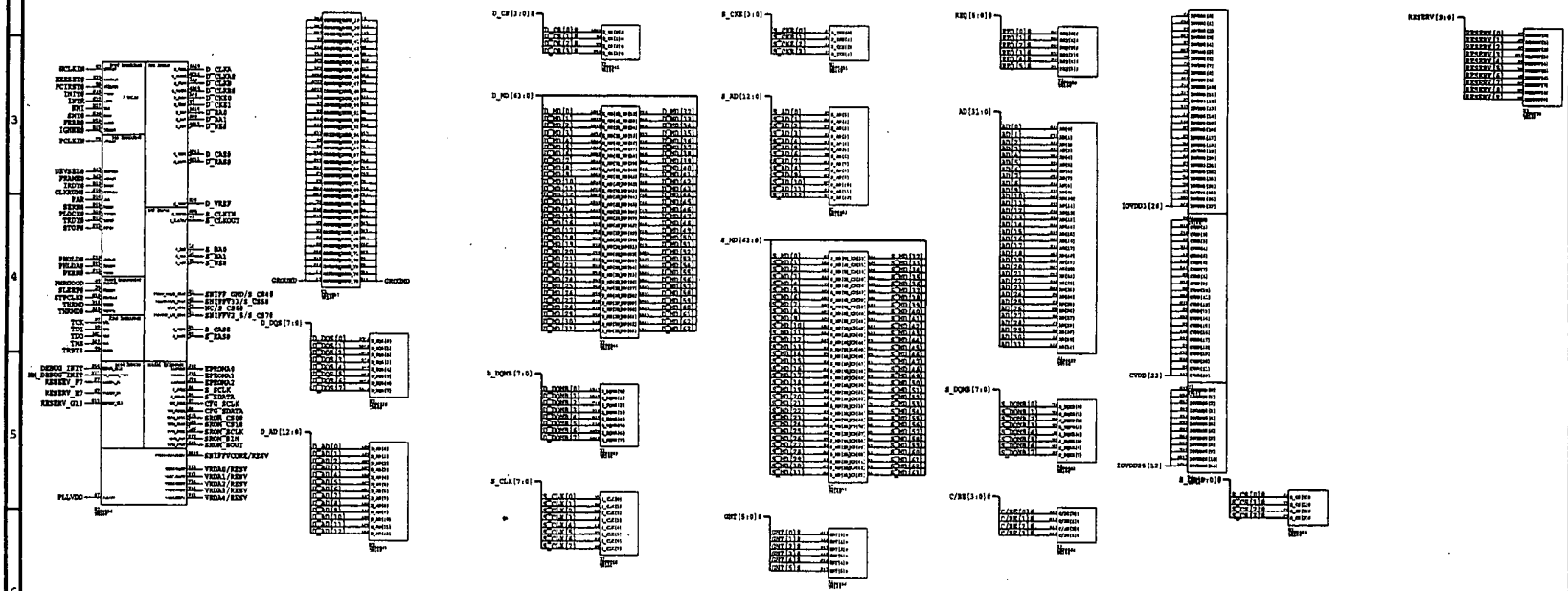
Page Title: Fiducials, Holes, Spare Gates



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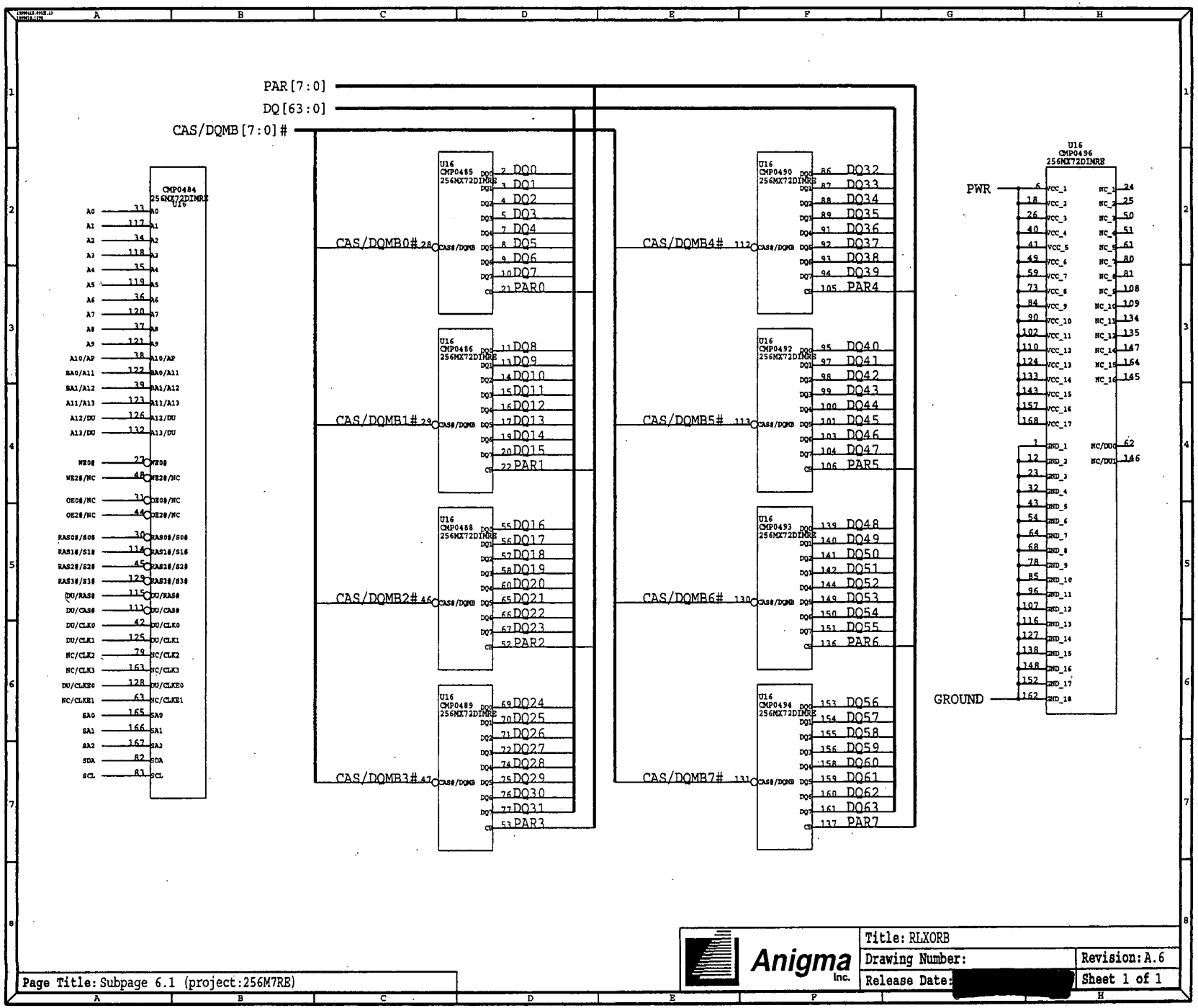
Page Title: Subpage 2.1 (project:TM160)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U16
CMP0493
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U16
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256MX72DIMRE
U16
CMP0496
256MX72DIMRE
CAS/DQMB0# 28
CAS/DQMB1# 29
CAS/DQMB2# 46
CAS/DQMB3# 47
CAS/DQMB4# 112
CAS/DQMB5# 113
CAS/DQMB6# 130
CAS/DQMB7# 131
PWR
GROUND
Anigma Inc.
Title: RLXORB
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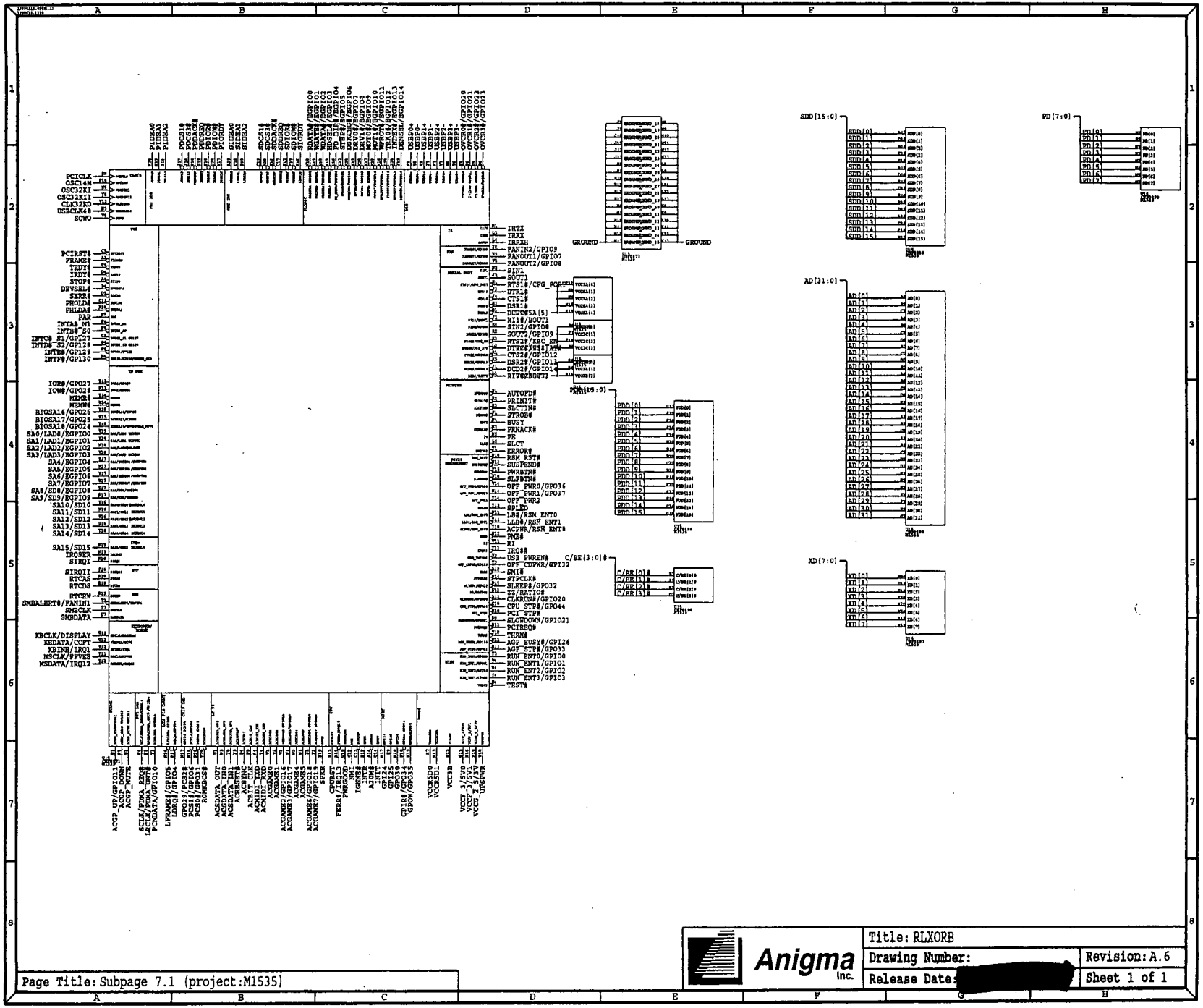
Page Title: Subpage 6.1 (project:256M7RB)



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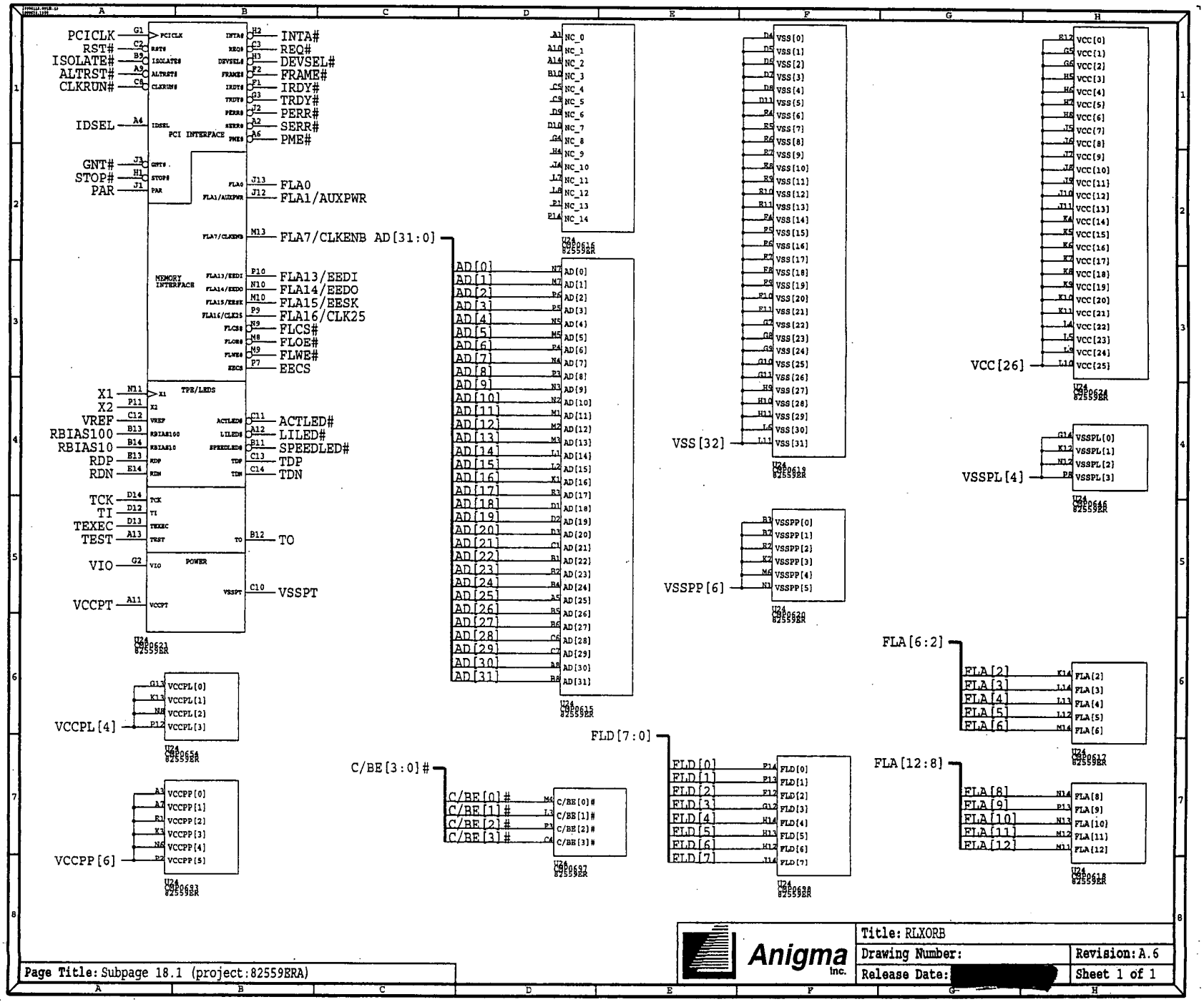
Page Title: Subpage 7.1 (project:M1535)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ISOLATE#
ALTRST#
CLKRUN#
IDSEL
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PAR
PCI INTERFACE
INTA#
REQ#
DEVSEL#
FRAME#
IRDY#
TRDY#
PERR#
SERR#
PME#
FLA0
FLA1/AUXPWR
FLA7/CLKENB
MEMORY INTERFACE
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16/CLK25
FLCS#
FLOE#
FLWE#
EECS
X1
X2
VREF
RBIAS100
RBIAS10
RDP
RDN
TPE/LEDS
ACTLED#
LILED#
SPEEDLED#
TDP
TDN
TCK
TI
TEXEC
TEST
TO
VIO
POWER
VCCPT
VSSPT
VCCPL[4]
VCCPP[6]
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C/BE[3:0]#
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VCC[26]
VSSPL[4]
FLA[6:2]
FLA[12:8]
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Title: RLXORB
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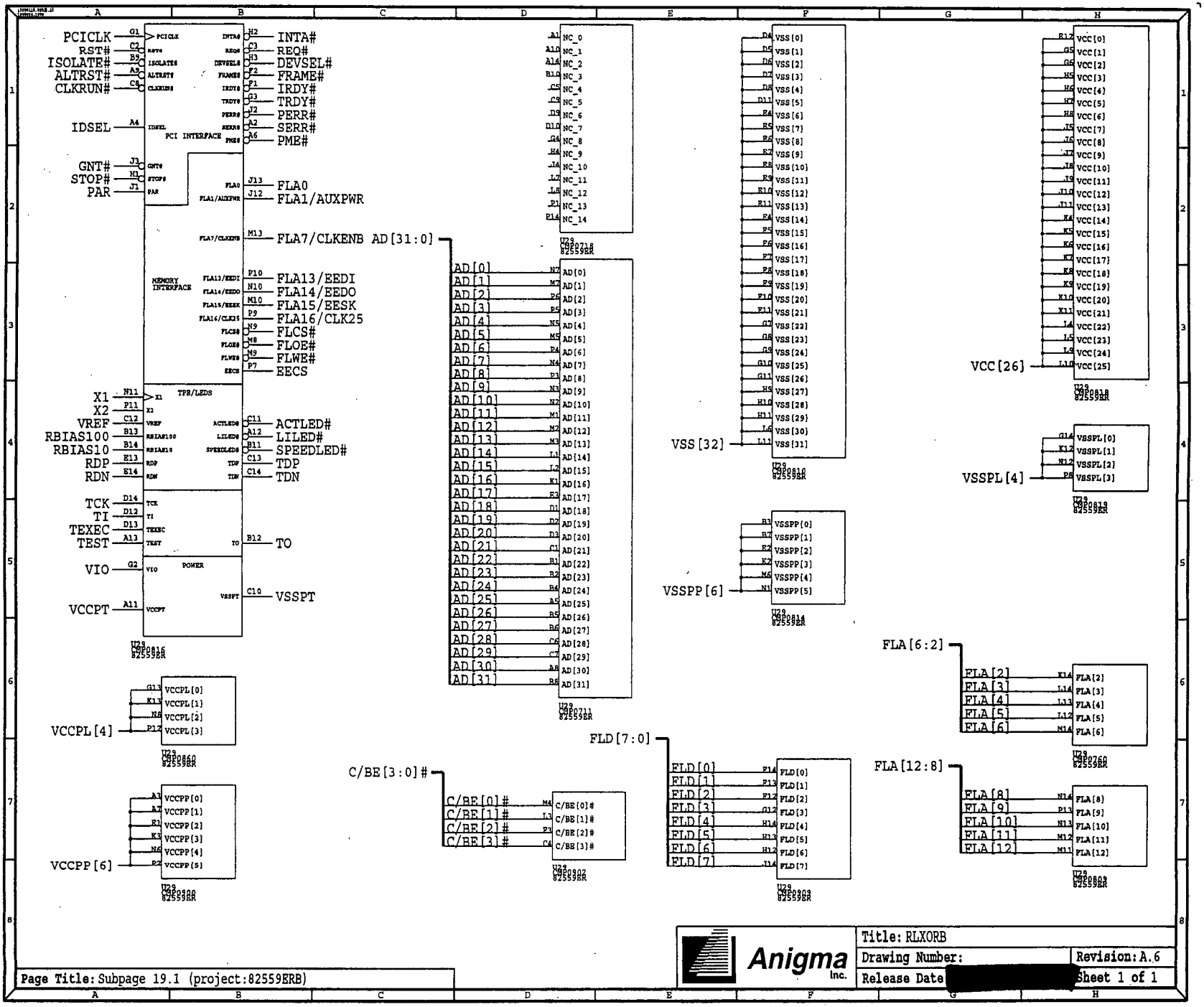
Page Title: Subpage 18.1 (project:82559ERA)



Page Title: Subpage 19.1 (project:82559ERB)	
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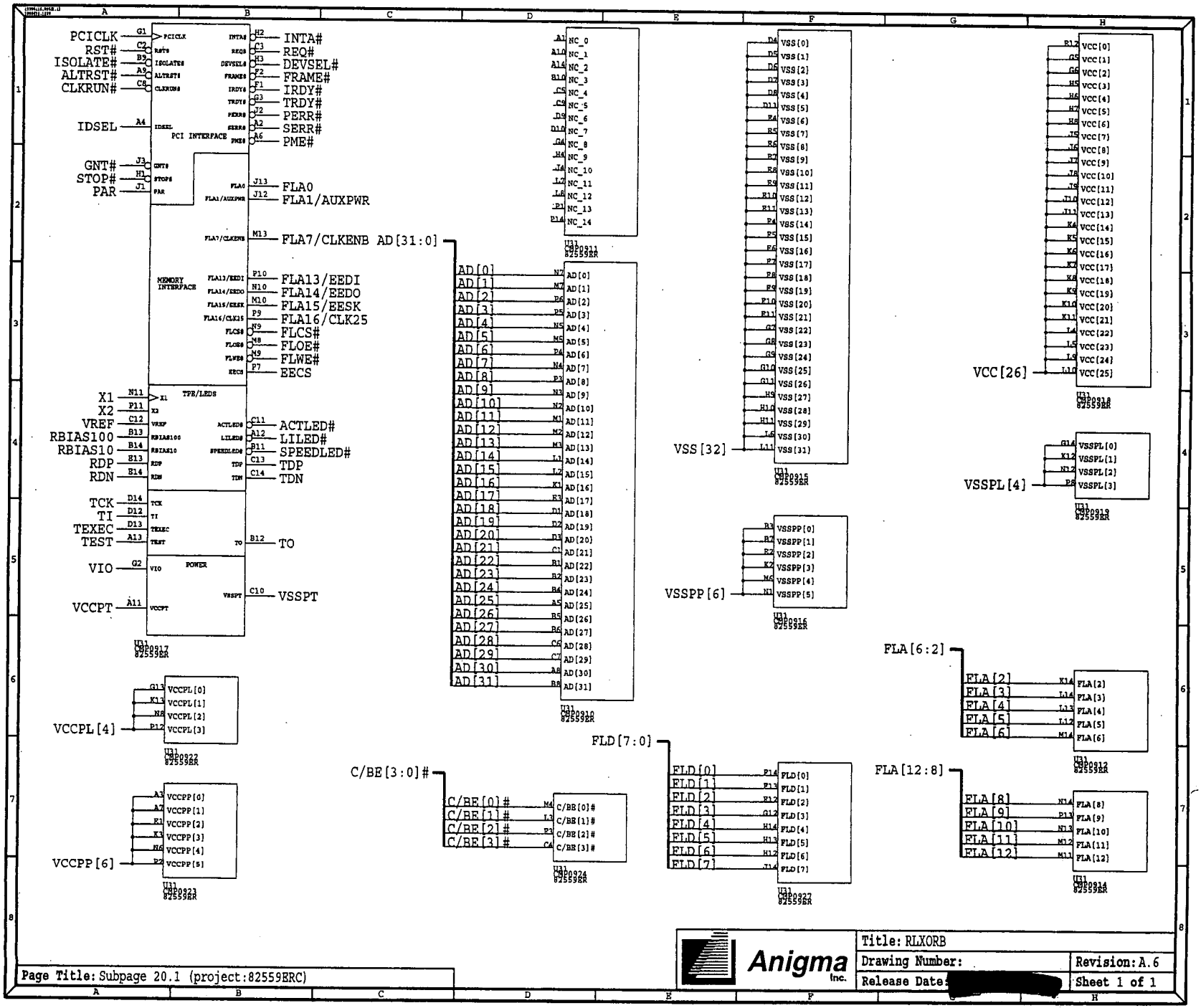

Anigma Inc.	Title: RLXORB
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